

# Jaguar-2 SVT Planar Logic Schematics

**JG2AL-6**  
**VER 2.23**  
**Dec/10/2021**

1.TITLE PAGE  
2.EC HISTORY  
3.CPU (1/16): DDI/TYPE-C  
4.CPU (2/16): DDR (1/2)  
5.CPU (3/16): DDR (2/2)  
6.CPU (4/16): MISC/JTAG  
7.CPU (5/16): ESPI/SPI/SMBUS/C-LINK  
8.CPU (6/16): LPSS/ISH  
9.CPU (7/16): AUDIO  
10.CPU (8/16): PCIE/USB/SATA  
11.CPU (9/16): CSI-2/CNVI  
12.CPU (10/16): CLOCK SIGNALS  
13.CPU (11/16): SYSTEM PM  
14.CPU (12/16): CPU POWER (1/2)  
15.CPU (13/16): CPU POWER (2/2)  
16.CPU (14/16): PCH POWER  
17.CPU (15/16): GND  
18.CPU (16/16): CFG/RESERVED  
19.ISFF\_DEBUG\_PORT  
20.RTC BATTERY  
21.SPI FLASH  
22.DISCRETE TPM 2.0  
23.LPDDR5 CHANNEL 0&1  
24.LPDDR5 CHANNEL 2&3  
25.LPDDR5 CHANNEL 4&5  
26.LPDDR5 CHANNEL 6&7  
27.LCD & TOUCH PANEL INTERFACE  
28.LID/CAMERA/MIC/SENSOR INTERFACE  
29.PEN CHARGER INTERFACE  
30.HDMI CONNECTOR  
31.THUNDERBOLT RETIMER F (1/2)  
32.THUNDERBOLT RETIMER F (2/2)  
33.THUNDERBOLT RETIMER R(1/2)  
34.THUNDERBOLT RETIMER R(2/2)  
35.USB PD CONTROLLER

36.THUNDERBOLT CONNECTOR F  
37.THUNDERBOLT CONNECTOR R  
38.M.2 SOCKET 3 MODULE I/F  
39.M.2 TYPE 1216 MODULE  
40.M.2 SOCKET 2 MODULE I/F  
41.USB TYPE-A CONNECTOR(1/2)  
42.USB TYPE-A CONNECTOR(2/2)  
43.BLANK  
44.BLANK  
45.BLANK  
46.BLANK  
47.BLANK  
48.BLANK  
49.BLANK  
50.BLANK  
51.BLANK  
52.BLANK  
53.BLANK  
54.BLANK  
55.AUDIO CODEC (ALC3306)  
56.AUDIO CONNECTOR  
57.AUDIO SMART AMP  
58.AUDIO SPEAKER  
59.AUDIO BEEP  
60.MEC1723 (1/4)  
61.MEC1723 (2/4)  
62.MEC1723 (3/4)  
63.MEC1723 (4/4)  
64.KEYBOARD & TRACK POINT  
65.TOUCH PAD/NFC/FPR  
66.PWR SW & FPR INTERFACE  
67.FAN CONNECTOR  
68.INTELLIGENT COOLING G-SENSOR  
69.ISH ACCELEROMETER  
70.THINK ENGINE 3 (1/2)

## BASE LOGIC :

Jaguar-1 SIT Planar Logic Scchematics Ver.2.15

71.THINK ENGINE 3 (2/2)  
72.BLANK  
73.DC INPUT  
74.BATTERY INPUT  
75.BATTERY CHARGER (BQ25710)  
76.DC/DC VCC5M (NB690)  
77.DC/DC VCC5\_PD (NB693A)  
78.DC/DC VCC3M (TPS51393P)  
79.LOAD SW VCC3\_SUS  
80.DC/DC VCC1R8\_SUS (TPS62827)  
81.DC/DC VCCPCHCORE(MP2961)  
82.DC/DC VCCPCHCORE DE\_CAP  
83.DC/DC VCC1R05A/1R8A/0R5A(NB705)  
84.DC/DC VCCCPUCORE (MP2964)  
85.DC/DC\_VCCCPUCORE(MP86941C)  
86.DC/DC VCCCPUCORE\_DE\_CAP  
87.LOAD SW VCC1R05\_PROC  
88.DC/DC VCCGFXCORE(MP86941C)  
89.LOAD SW B  
90.BLANK  
91.VNN\_VCC1R05\_BYPASS(NB695A)  
92.BLANK  
93.BLANK  
94.BLANK  
95.LOAD SW TOUCH PANEL & SSD  
96.PTH FOR SCREW HOLES  
97.BLANK  
98.BLANK

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Project Name : Jaguar-2	Title : TITLE PAGE	
Size : C	Document Number :	Rev : 2.23
Date: Friday, December 10, 2021		Sheet : 1 of 98

## EC HISTORY

JG2AL-6

(Base Logic : Jaguar-1 SIT Planar Logic Schematic Ver 2.15)

VER.2.21 2021/11/25 APPLIED JG2\_SVT\_EC001-EC008

VER.2.21 2021/11/25 APPLIED JG2\_SVT\_EC001-EC008

VER.2.22 2021/11/29 APPLIED JG2\_SVT\_EC009-EC010

VER.2.23 2021/12/10 APPLIED JG2\_SVT\_EC011

### LCFC 3Pin Symbol rule

#### Orcad Symbol & PCB Footprint pin assignment

Use common rule, Top side is Pin1, not follow original datasheet definition to avoid confusion with different vender definition. Below is an example.

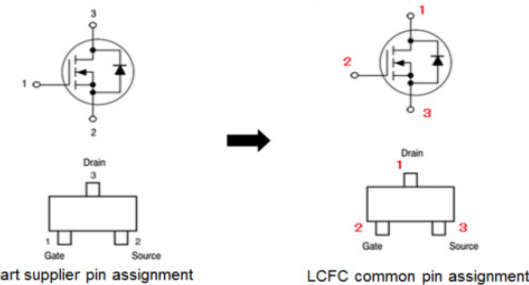


TABLE: Chip Capacitor Thermal Characteristics

		Code
-55 to 150degC	+/-30ppm/degC	NPO
-55 to 125degC	+/-30ppm/degC	C0G
-55 to 125degC	+/-15%	X7R
-55 to 105degC	+/-22%	X6S
-55 to 85degC	+/-15%	X5R

TABLE: Chip Capacitor Tolerance

Tolerance	Code
+/-0.1pF	B
+/-0.25pF	C
+/-0.5pF	D
+/-5%	J
+/-10%	K
+/-20%	M
+80/-20%	Z

TABLE: Chip Part Dimension

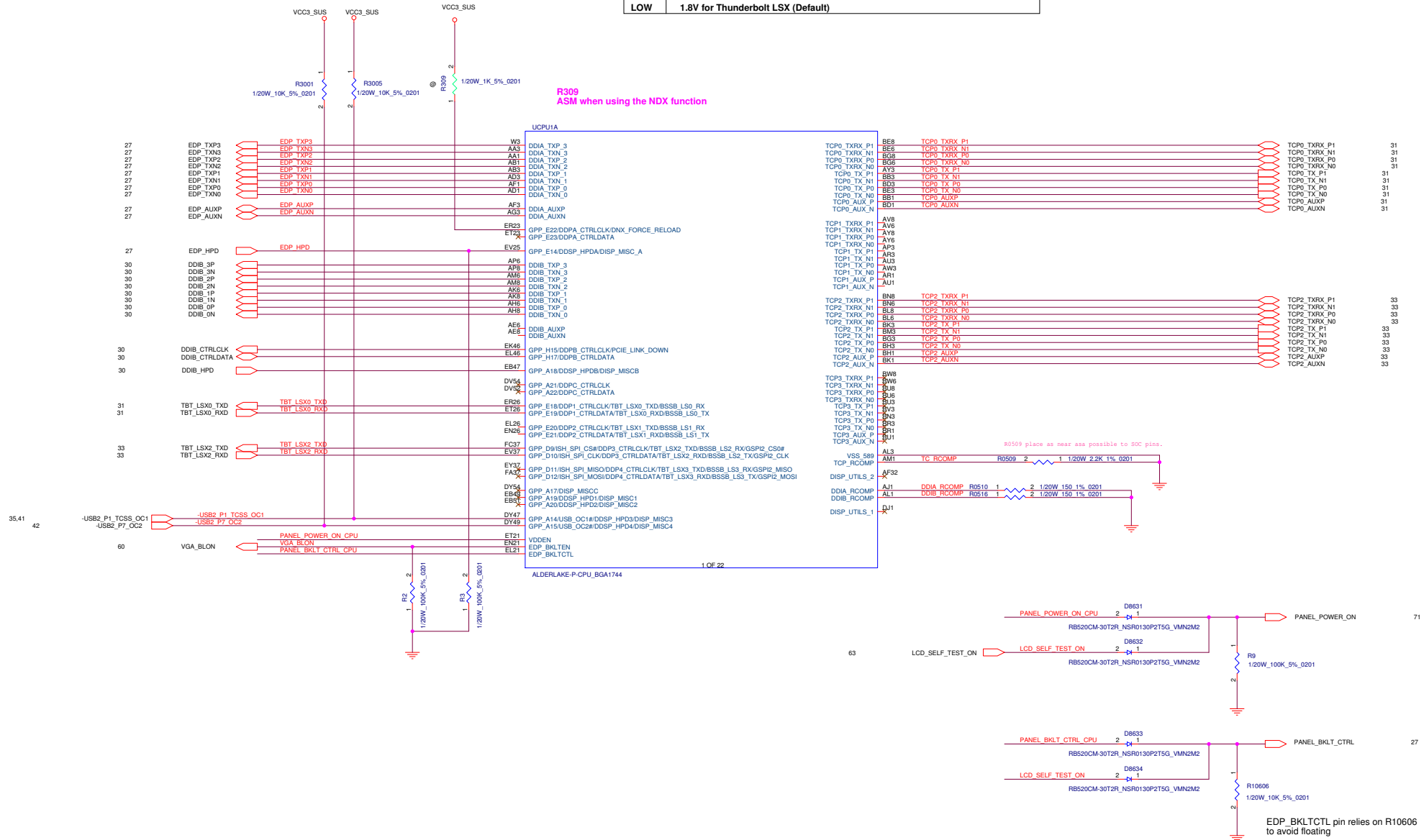
Size [mm]	mm Size Code	Inch Size Code
0.40 x 0.20	0402	01005
0.60 x 0.30	0603	0201
1.00 x 0.50	1005	0402
1.60 x 0.80	1608	0603
2.00 x 1.25	2125	0805
2.00 x 1.60	2016	0806
2.50 x 2.00	2520	1008
3.20 x 1.60	3216	1206
3.20 x 2.50	3225	1210
4.50 x 1.60	4516	1806
4.50 x 2.50	4525	1810
4.50 x 3.20	4532	1812
5.00 x 2.50	5025	2010
6.40 x 3.20	6432	2512

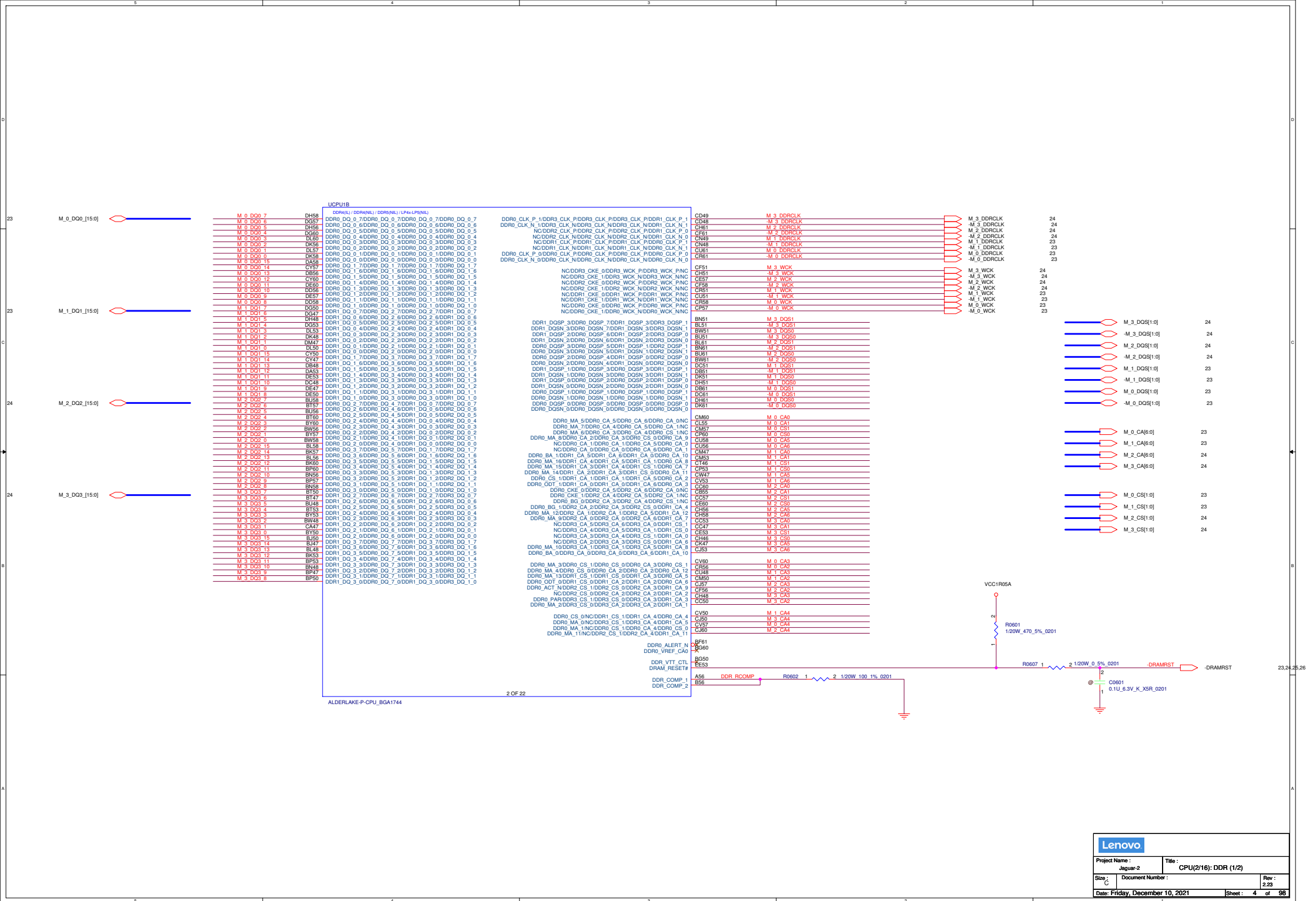
↑  
LOGIC

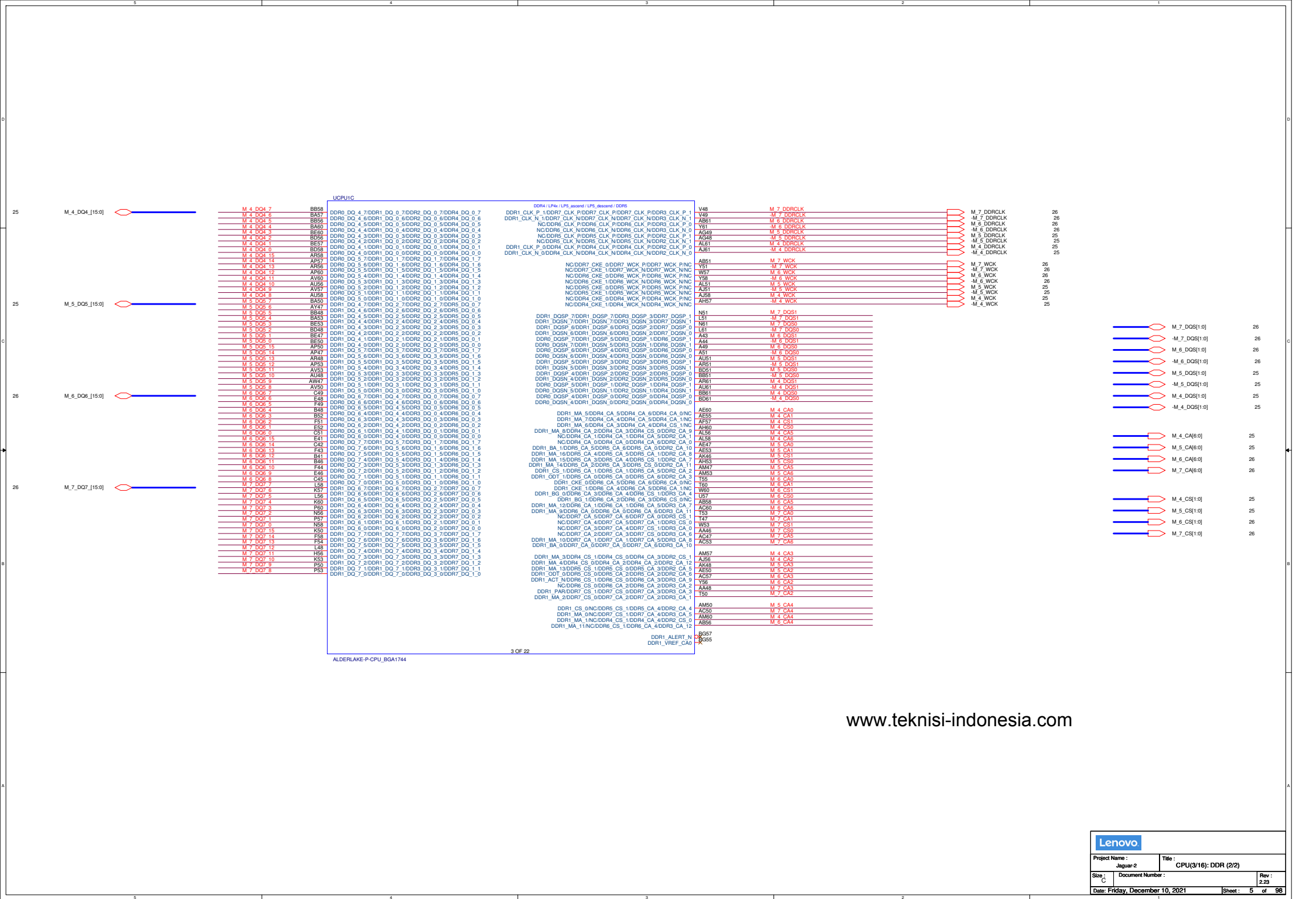
Lenovo			
Project Name : Jaguar-2		Title : EC HISTORY	
Size : C	Document Number :		Rev : 2.23
Date: Friday, December 10, 2021		Sheet : 2	of 98

TABLE : Functional Strap

GPP_E19/DDP1_CTRLDATA/TBT_LXS0_RXD (DDP1 I2C / TBT_LXS0 Pin VCC Configuration)
GPP_E21/DDP2_CTRLDATA/TBT_LXS1_RXD (DDP2 I2C / TBT_LXS1 Pin VCC Configuration)
GPP_D10/DDP3_CTRLDATA/TBT_LXS2_RXD (DDP3 I2C / TBT_LXS2 Pin VCC Configuration)
GPP_D12/DDP4_CTRLDATA/TBT_LXS3_RXD (DDP4 I2C / TBT_LXS3 Pin VCC Configuration)
HIGH 3.3V for HDMI Display I2C (External Pull-Up Resistor Required)
LOW 1.8V for Thunderbolt LSX (Default)







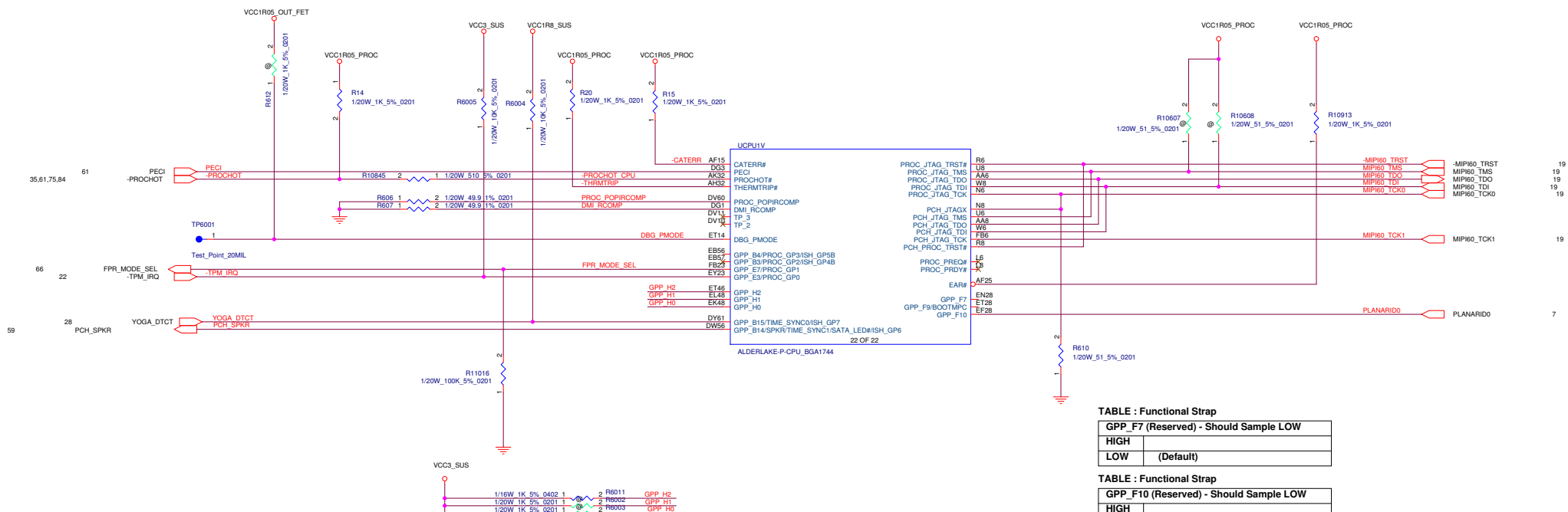


TABLE : Functional Strap

DBG_PMODE (DFx Test Mode)	
HIGH	DFx Test Mode Disabled (default)
LOW	DFx Test Mode Enabled

TABLE : Functional Strap

GPP_F7 (Reserved) - Should Sample LOW	
HIGH	
LOW	(Default)

TABLE : Functional Strap

GPP_F10 (Reserved) - Should Sample LOW	
HIGH	
LOW	(Default)

TABLE : Functional Strap		
SPI0_MOSI (Boot Halt)		
HIGH	Disabled	
LOW	Enabled	

TABLE : Functional Strap

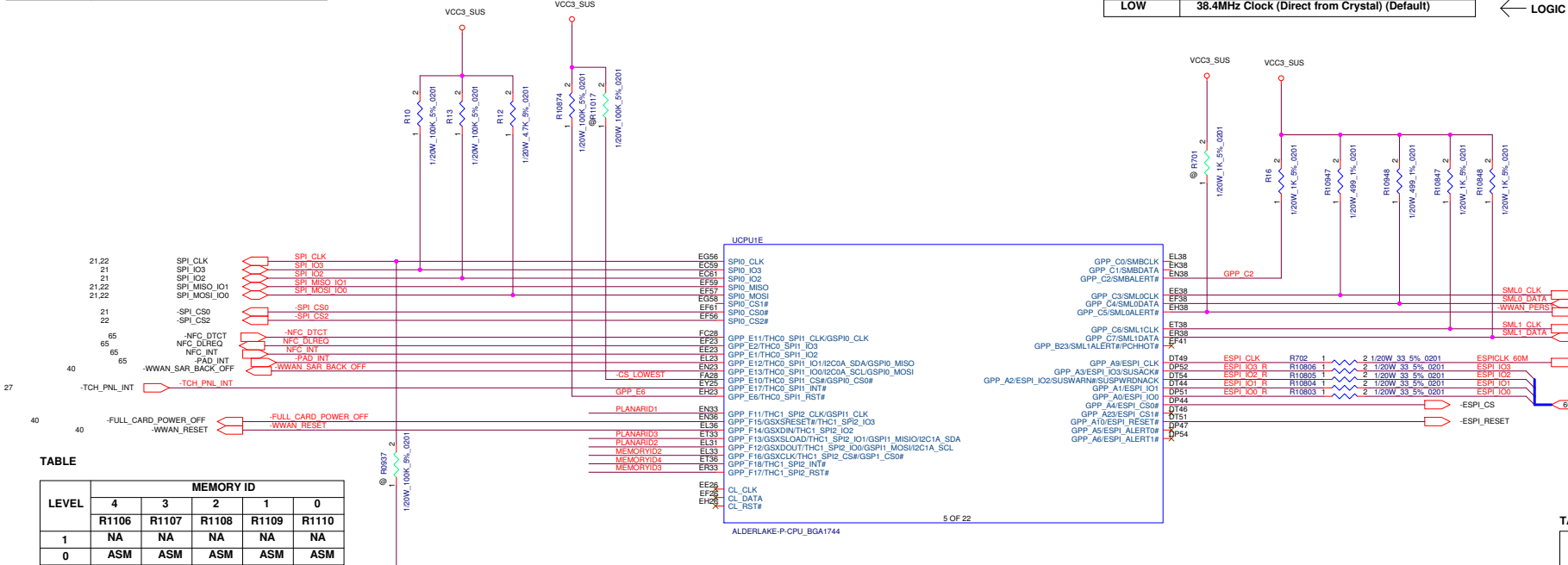
SPI0_IO2 (Consent Strap)		
HIGH	Disabled	
LOW	Enabled	

TABLE : Functional Strap

SPI0_IO3 (A0 Personality Strap)		
HIGH	Disabled	
LOW	Enabled	

TABLE : Functional Strap

GPP_E6 (JTAG ODT Disable)		
HIGH	JTAG ODT Enabled	
LOW	JTAG ODT Disabled	



TABLE

LEVEL	MEMORY ID				
	4	3	2	1	0
1	NA	NA	NA	NA	NA
0	ASM	ASM	ASM	ASM	ASM

TABLE:

MEMORYID[4:0]	U2501,U2601,U2701,U2801				Total Memory
	Supplier	Supplier's P/N	Capacity	DDP	
00h (00000b)	SK hynix	H9JCNNNBK3MLYR-N6E	16Gbit	DDP	8GB
04h (00100b)		H9JCNNNCP3MLYR-N6E	32Gbit	QDP	16GB
08h (01000b)		H9JCNNNFA5MLYR-N6E	64Gbit	ODP	32GB
0Ch (01100b)	Samsung	K3LKBK80BM-MGCP	32Gbit	DDP	16GB
10h (10000b)		K3LKCKC0BM-MGCP	64Gbit	QDP	32GB
14h (10100b)		MT62F512M32D2DR-031 WT:B	16Gbit	DDP	8GB
18h (11000b)	Micron	MT62F1G32D4DR-031 WT:B	32Gbit	QDP	16GB
1Ch (11100b)		MT62F2G32D8DR-031 WT:B	64Gbit	ODP	32GB

TABLE

LEVEL	PLANAR ID				
	R1102	R1103	R1104	R1105	
1	NA	NA	NA	NA	
0	ASM	ASM	ASM	ASM	

TABLE

LEVEL	PLANARID[3:0]
EVT	0000B
ME-FVT	0001B
EE-FVT	0010B
ME-SIT	0011B
EE-SIT	0100B
ME-SIT-R	0101B
MFG-SIT-R	0110B
SVT	0111B

TABLE : Functional Strap

GPP_B14/SPKR (Top Swap Override)	
HIGH	Enable "Top Swap" mode
LOW	Disable "Top Swap" mode (Default)

LOGIC

ISH I2C0: 1.8V

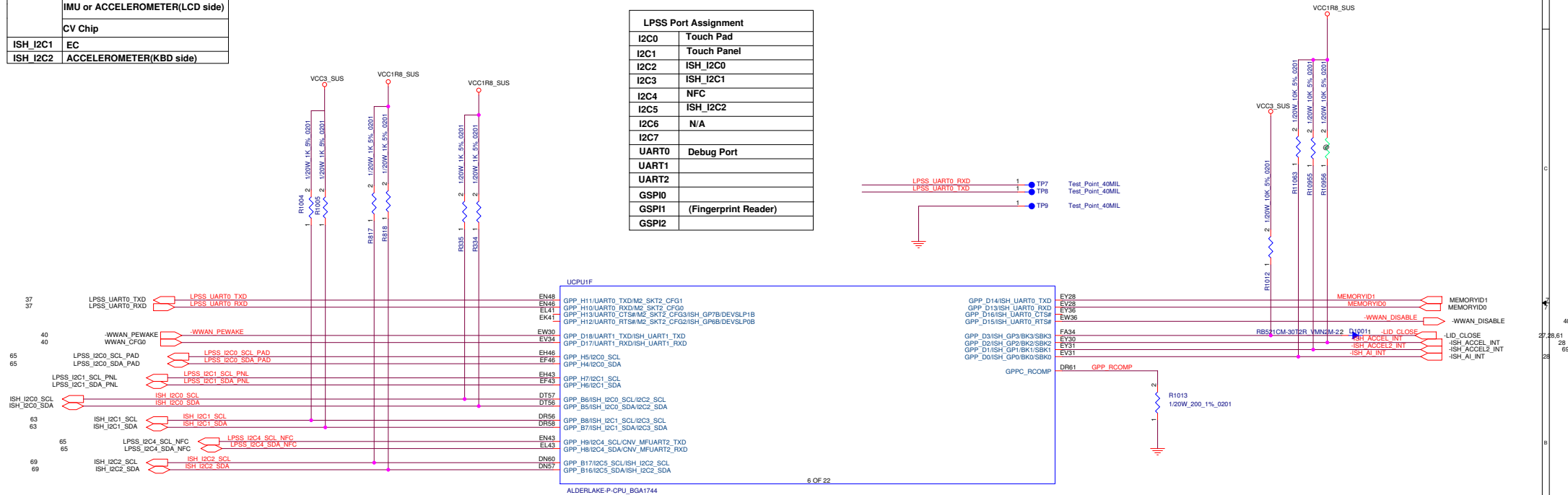
ISH I2C1: 3.3V

TABLE: ISH I2C Port Assignment

ISH_I2C0	ACCELEROMETER
	IMU or ACCELEROMETER(LCD side)
	CV Chip
ISH_I2C1	EC
ISH_I2C2	ACCELEROMETER(KBD side)

LPSS Port Assignment

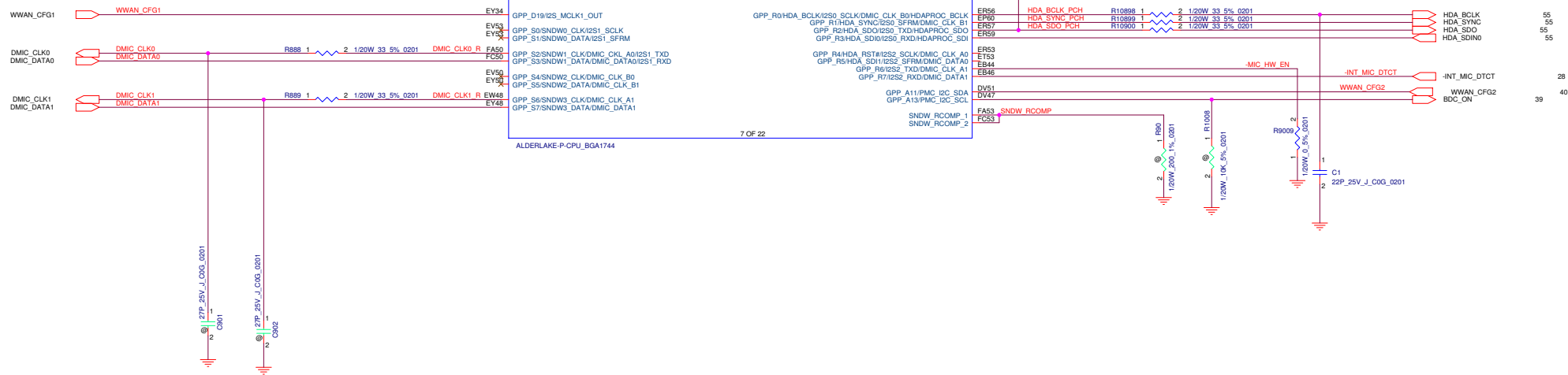
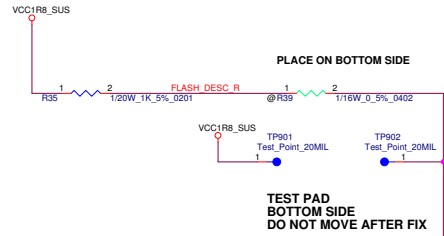
I2C0	Touch Pad
I2C1	Touch Panel
I2C2	ISH_I2C0
I2C3	ISH_I2C1
I2C4	NFC
I2C5	ISH_I2C2
I2C6	N/A
I2C7	
UART0	Debug Port
UART1	
UART2	
GSPi0	
GSPi1	(Fingerprint Reader)
GSPi2	



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Project Name : Jaguar-2		Title : CPU (6/16): LPSS/ISH	
Size :	Document Number :	Rev : 2.23	
Date: Friday, December 10, 2021		Sheet : 8	of 98

TABLE : Functional Strap	
GPP_R2/HDA_SDO/I2S0_TXD	
Flash Descriptor Security Override	
HIGH	Disable Flash Descriptor Security (Override)
LOW	Enable Flash Descriptor Security (Default)

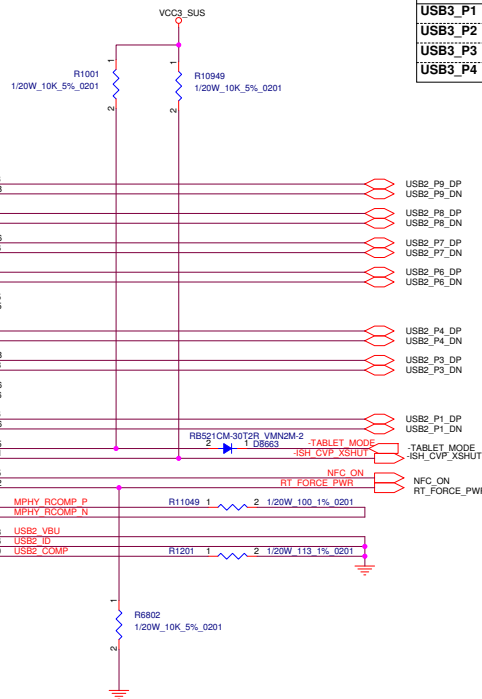
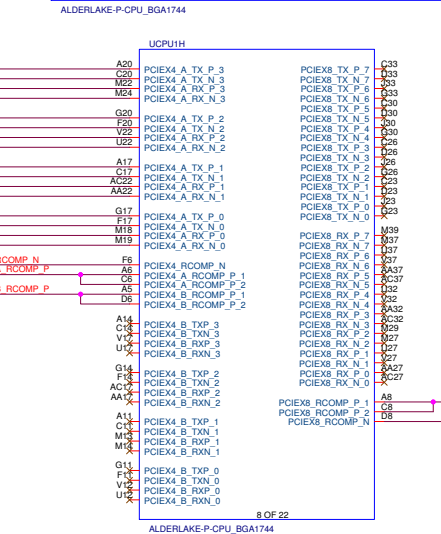
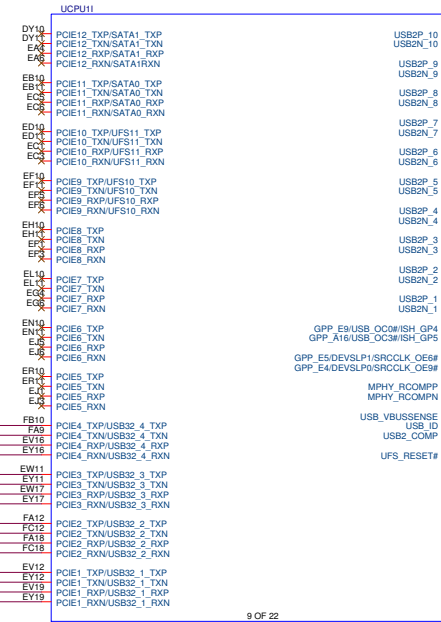
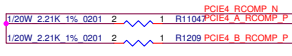
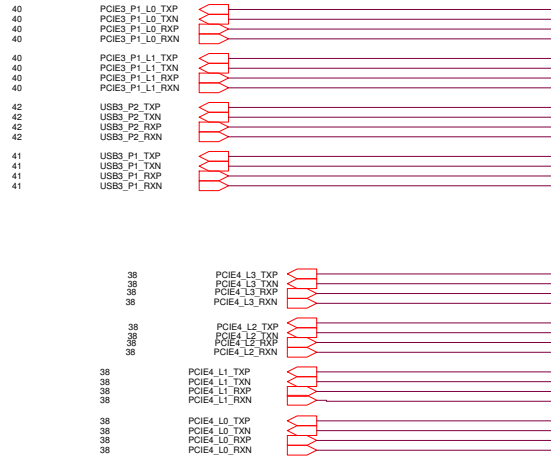


Flexible I/O Configuration								
HSIO Port	High Speed Signals	PCI		HSIO Configuration	Descriptor for PCIe	Net Name	PCI	
		Device	Function				Device	Function
PCH L0	USB 3.2 #1 / PCIe Gen3 #1	1Ch	0h	USB 3.2 #1	1x2, 2x1 Lane Reversal Enabled	USB3_P1	14h	0h
PCH L1	USB 3.2 #2 / PCIe Gen3 #2		1h	USB 3.2 #2		USB3_P2		
PCH L2	USB 3.2 #3 / PCIe Gen3 #3		2h	PCIe Gen3 #3		PCIE3_P1_L1		
PCH L3	USB 3.2 #4 / PCIe Gen3 #4		3h	PCIe Gen3 #4		PCIE3_P1_L0	1Ch	0h
PCH L4	PCIe Gen3 #5	1Ch	4h	PCIe Gen3 #5	4x1 Lane Reversal Disabled	PCIE3_P5	1Ch	4h
PCH L5	PCIe Gen3 #6		5h	PCIe Gen3 #6		N/A		
PCH L6	PCIe Gen3 #7		6h	PCIe Gen3 #7		N/A		
PCH L7	PCIe Gen3 #8		7h	PCIe Gen3 #8		N/A		
PCH L8	PCIe Gen3 #9 (GbE)	1Dh	0h	PCIe Gen3 #9 (x4)	1x4 Lane Reversal Disabled	N/A		
PCH L9	PCIe Gen3 #10		1h	PCIe Gen3 #10 (x4)		N/A		
PCH L10	PCIe Gen3 #11 / SATA #0		2h	PCIe Gen3 #11 (x4)		N/A		
PCH L11	PCIe Gen3 #12 / SATA #1		3h	PCIe Gen3 #12 (x4)		N/A		
CPU L0	PCIe Gen4 x4Lane 0	06h		PCIe Gen4 (x4) L0	1x4 Lane Reversal Disabled	PCIE4_L0		
CPU L1	PCIe Gen4 x4Lane 1			PCIe Gen4 (x4) L1		PCIE4_L1	06h	0h
CPU L2	PCIe Gen4 x4Lane 2			PCIe Gen4 (x4) L2		PCIE4_L2		
CPU L3	PCIe Gen4 x4Lane 3			PCIe Gen4 (x4) L3		PCIE4_L3		

PCIe Port Assignment	
PCIE3_P1	(USB3_P1)
PCIE3_P2	(USB3_P2)
PCIE3_P3	WWAN Lane 1
PCIE3_P4	WWAN Lane 0
PCIE3_P5	(WLAN)
PCIE3_P6	(Reserved)
PCIE3_P7	(GbE PHY)
PCIE3_P8	(SD Card)
PCIE3_P9 (x4)	(dGPU)
PCIE4 (x4)	NVMe SSD

SATA Port Assignment	
SATA_P0	(PCIE3_P11)
SATA_P1	(PCIE3_P12)

USB 2.0 Port Assignment	
USB2_P1	Type-C Port A
USB2_P2	(Reserved)
USB2_P3	Type-C Port C
USB2_P4	WWAN
USB2_P5	(Reserved)
USB2_P6	Fingerprint Reader
USB2_P7	Type-A Port (AOU)
USB2_P8	Camera MCU/ USB Camera
USB2_P9	Type-A Port (DCI)
USB2_P10	(Reserved)



USB 3.1 Port Assignment	
USB3_P1	Type-A Port (DCI)
USB3_P2	Type-A Port (AOU)
USB3_P3	(PCIE3_P3)
USB3_P4	(PCIE3_P4)

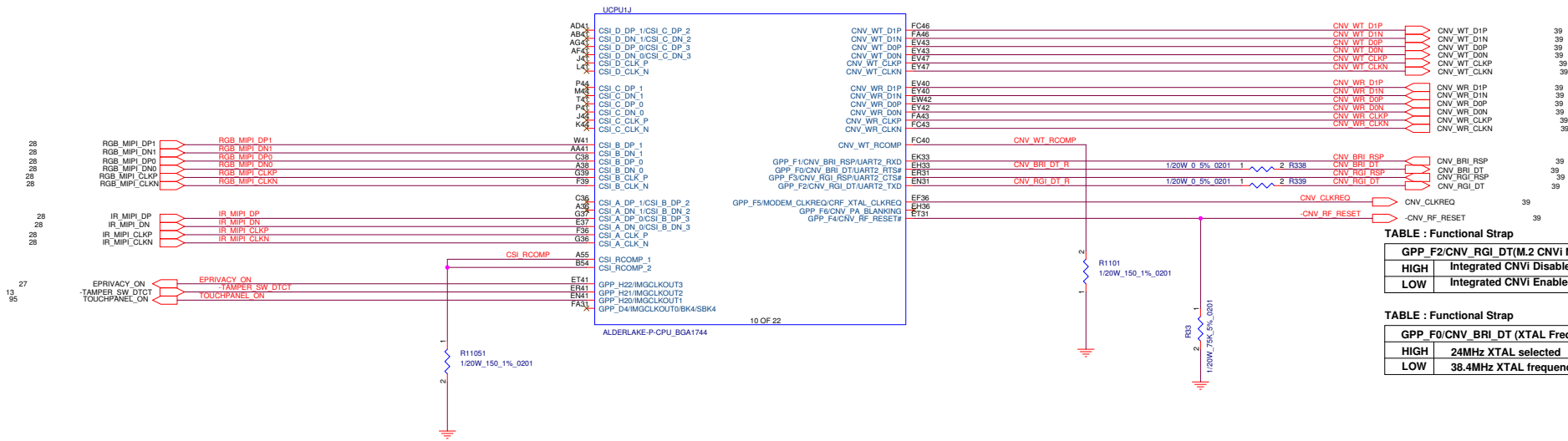


TABLE : Functional Strap

GPP_F2/CNV_RGI_DT(M.2 CNVi Mode Select)	
HIGH	Integrated CNVi Disabled
LOW	Integrated CNVi Enabled

← LOGIC

TABLE : Functional Strap

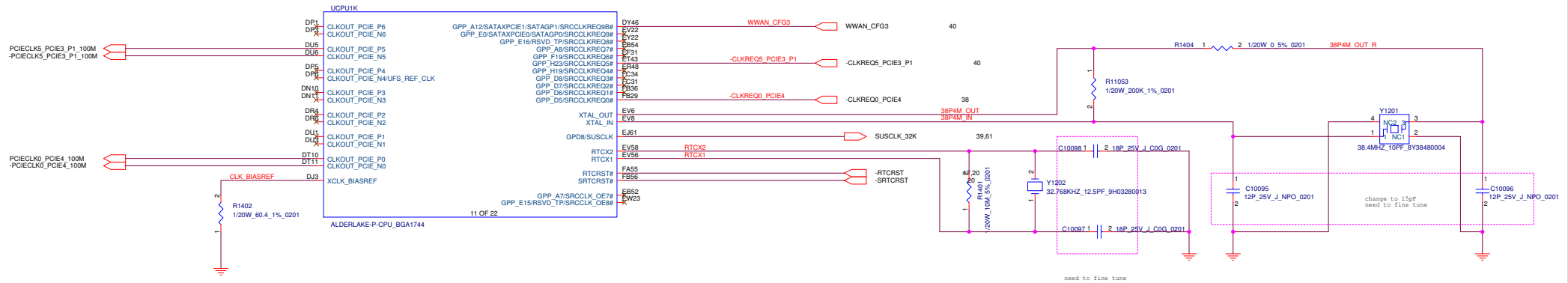
GPP_F0/CNV_BRI_DT (XTAL Frequency Selection)	
HIGH	24MHz XTAL selected
LOW	38.4MHz XTAL frequency selected (Default)

← LOGIC

PCIeCLK and CLKREQ# Port Assignment		
Port 0	PCIe Gen4 (x4)	NVMe SSD
Port 1	PCIe Gen3 P8	(SD Card)
Port 2	PCIe Gen3 P5	(M.2 WLAN)
Port 3	PCIe Gen3 P9 (x4)	(dGPU)
Port 4	PCIe Gen3 P7	(GbE PHY)
Port 5	PCIe Gen3 P1	M.2 WWAN
Port 6	PCIe Gen3 P6	(Reserved)

TABLE of Y1202		
Vendor	P/N	LCFC P/N
TXC	9H03280013	SJ100011T00
KDS	7BD03276A2S	SJ100011W00
EPSON	X1A0001410003	SJ10000LM00

TABLE of Y1201		
Vendor	P/N	LCFC P/N
TXC	8Y38480004	SJ10000SN00
KDS	7AF03840A04	SJ10000XG00
MURATA	XRCGB38M400F2T10R0	SJ100012100

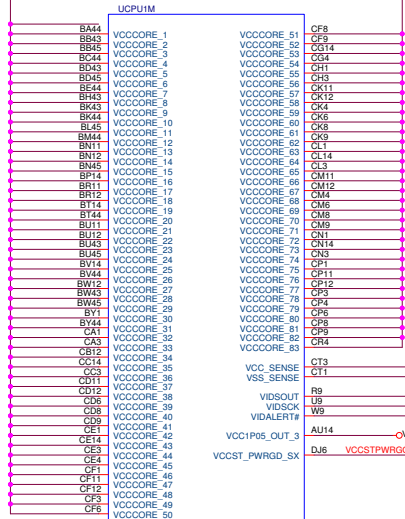
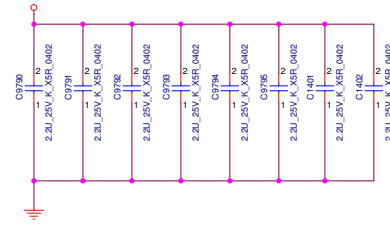




VCCCPUCORE

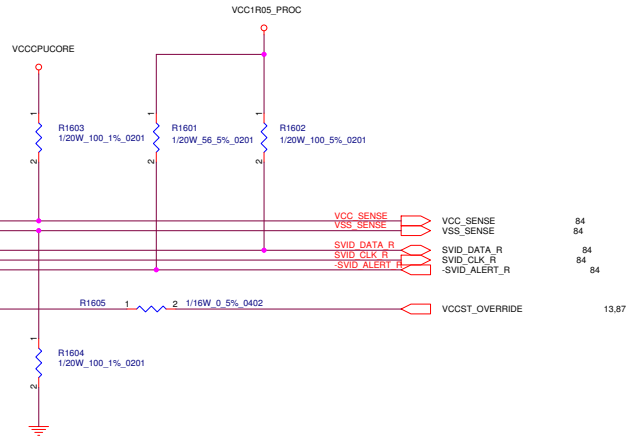
VCCCPUCORE

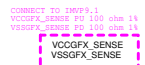
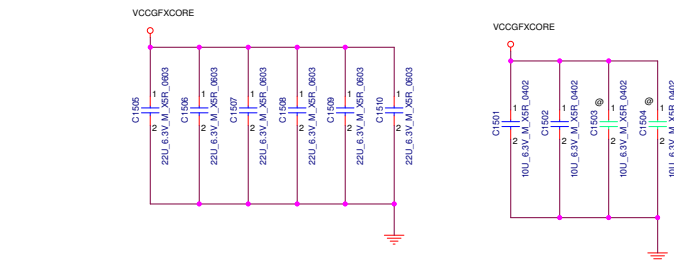
VCCCPUCORE

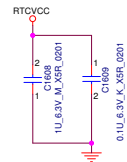
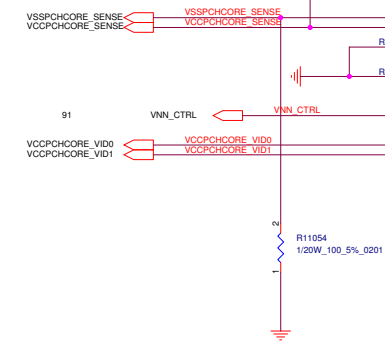
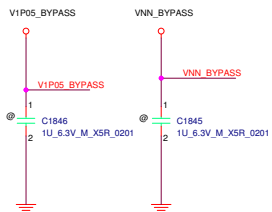
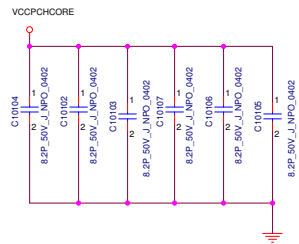
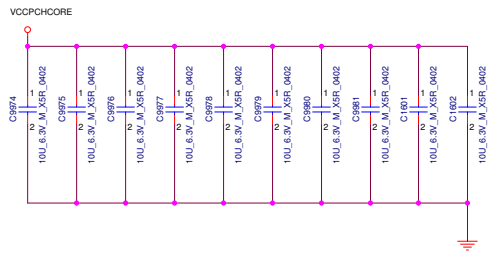


13 OF 22

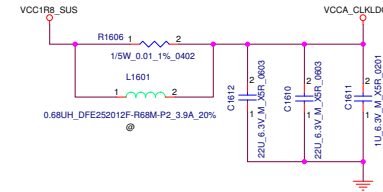
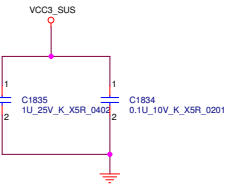
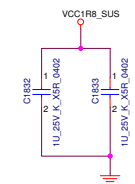
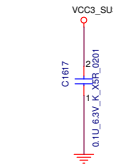
ALDERLAKE-P-CPU\_BGA1744



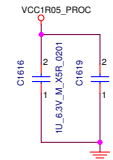




Please as close to the pin EB42



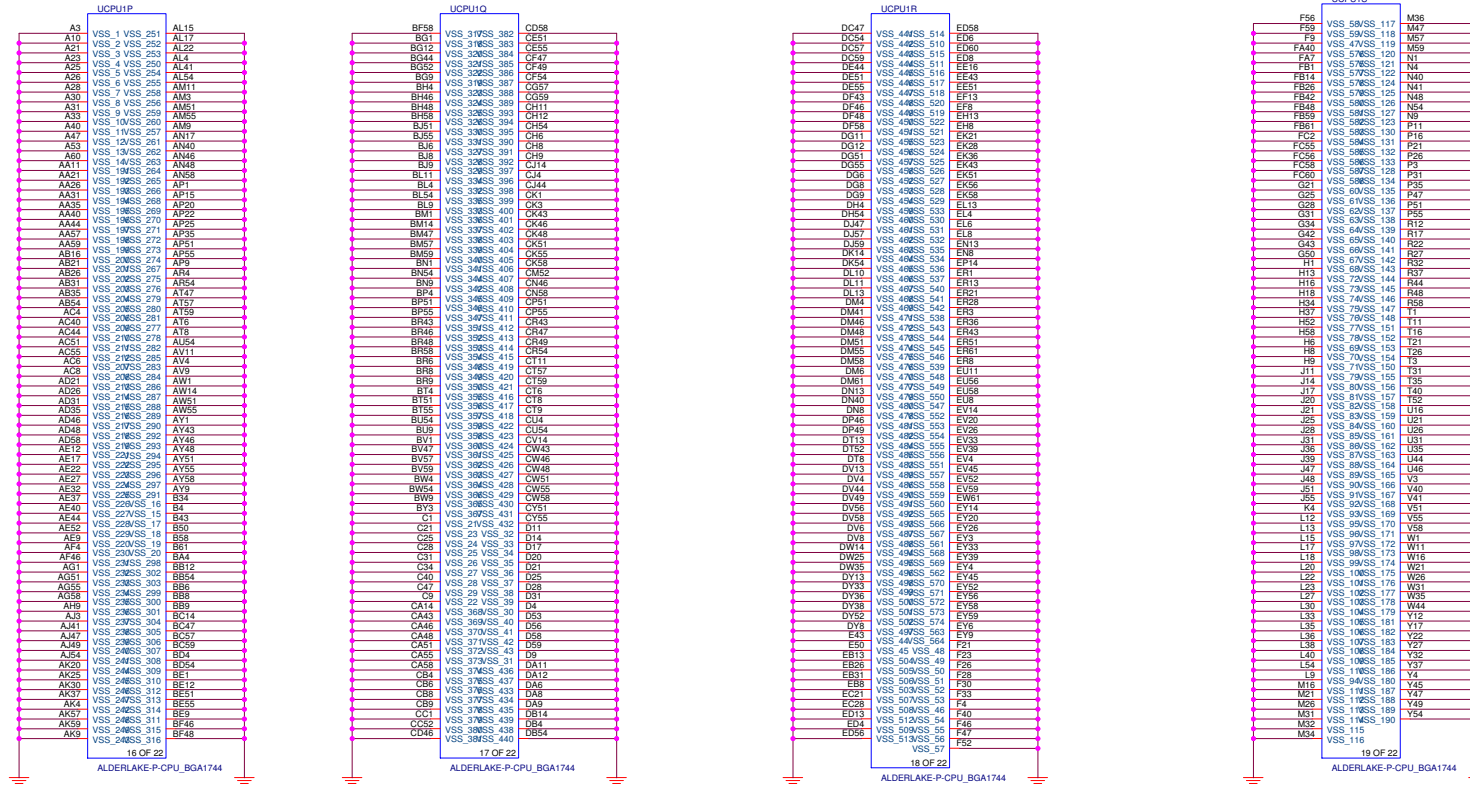
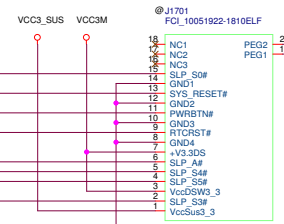
teknisi-indonesia.com



Place as close to the Pin EU4,EU1

Intel 80 Audio Supply. Can operate at 3.3V or 1.8V. VCC1R05 can be swapped directly to either VCC1R05\_1P8 or VCC1R05\_1P8 power plane depending on the operating voltage. Required immediate ground reference for VCC1R05 power plane.

# APS/PETS Interface

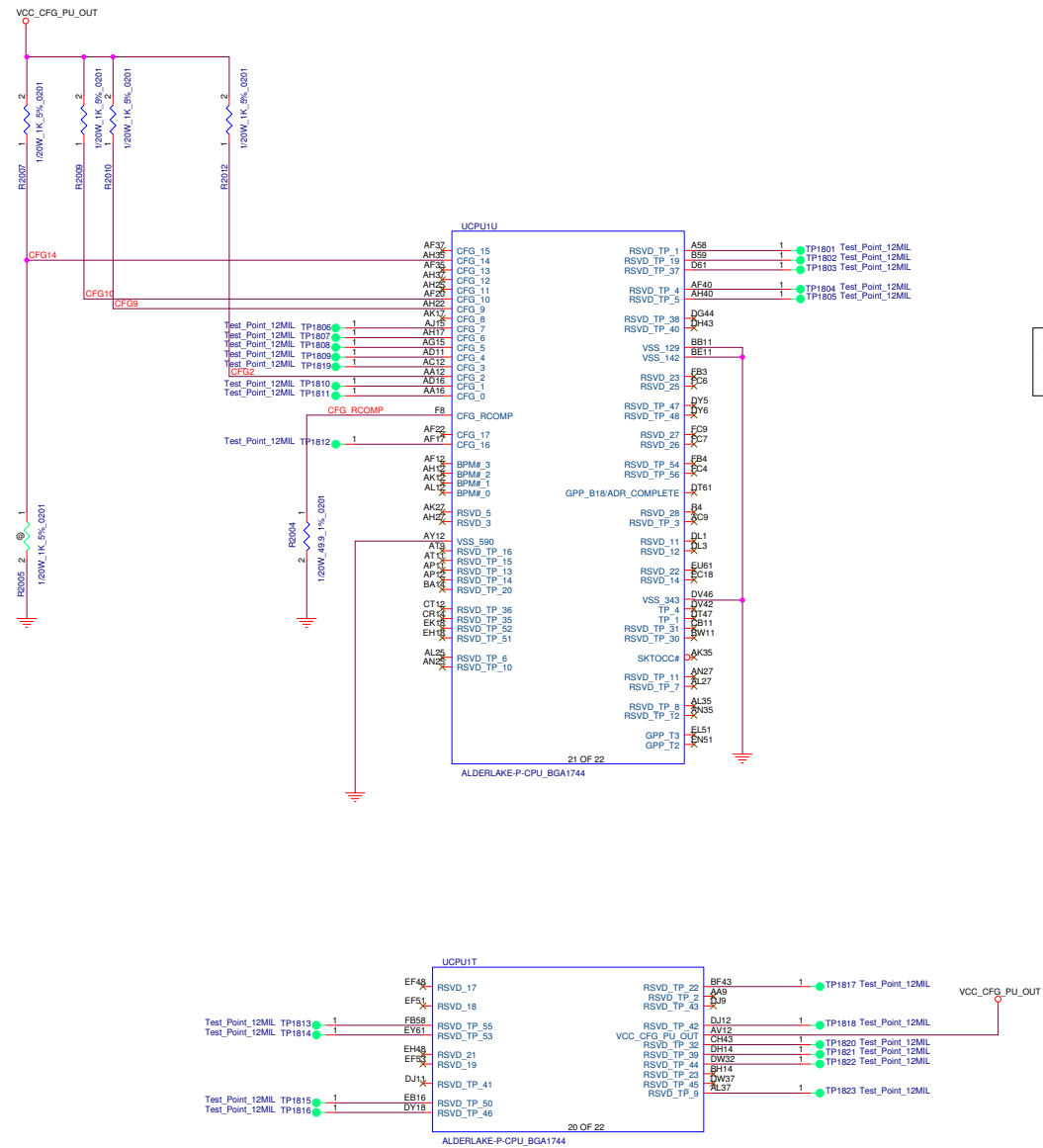


TABLE

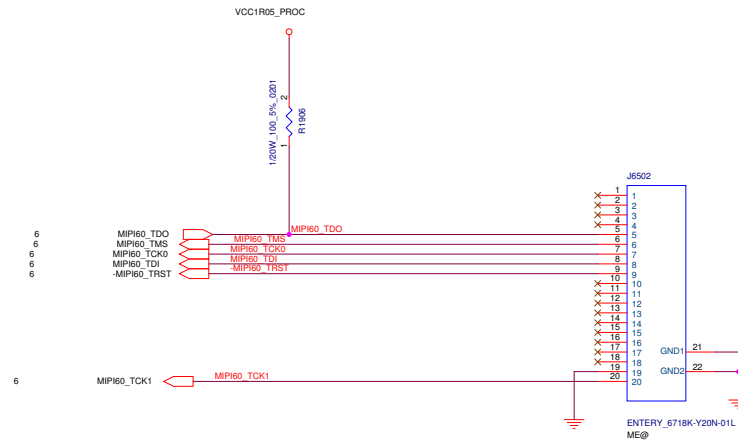
CFG14: PEG60 Lane Reversal

1:Normal

0:Reversed



ADR\_COMPLETE  
1:Enabled NO REBOOT  
0:Disabled REBOOT ENABLED

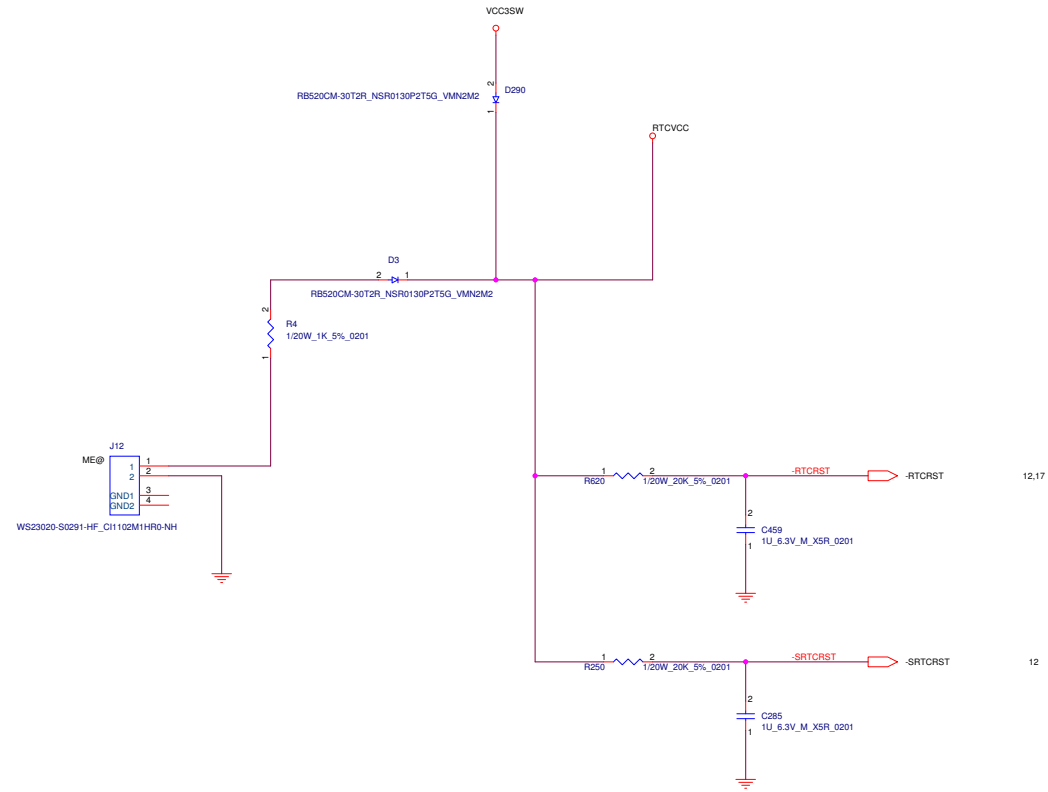


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TABLE

Logic	Ref Des	MIPI60	DCI2.0
page6	R612	ASM	NO ASM
	R10607	ASM	NO ASM
	R10608	ASM	NO ASM
page13	R1309	ASM	ASM
page19	R1906	ASM	ASM

↑  
LOGIC



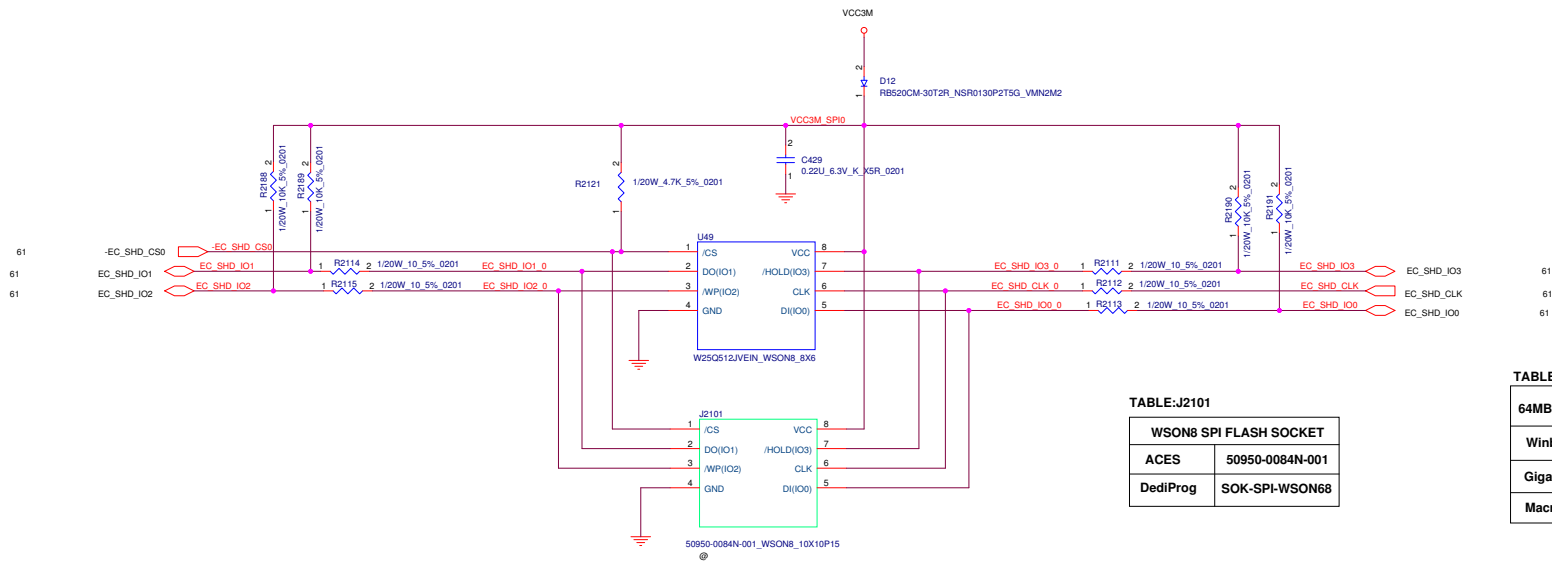
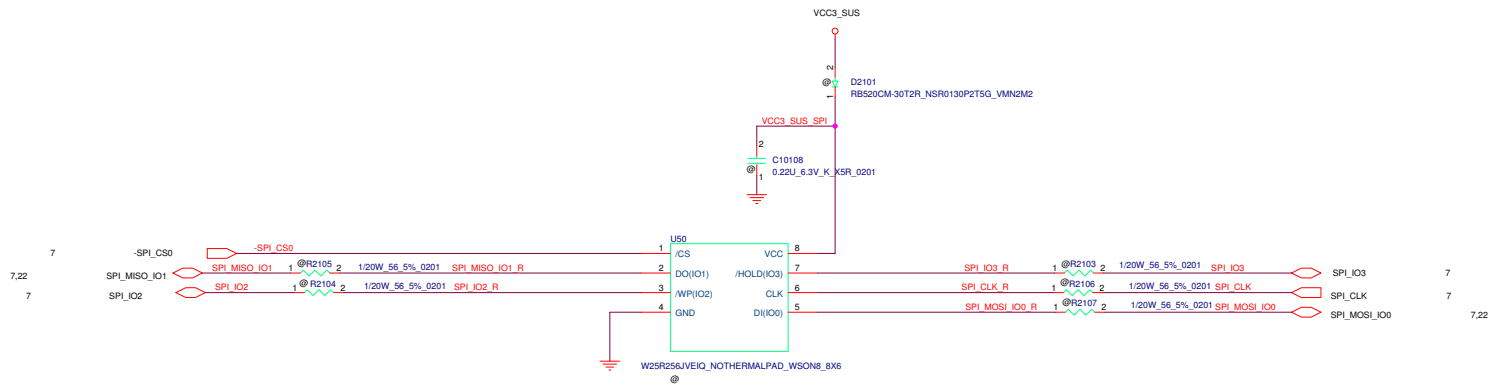
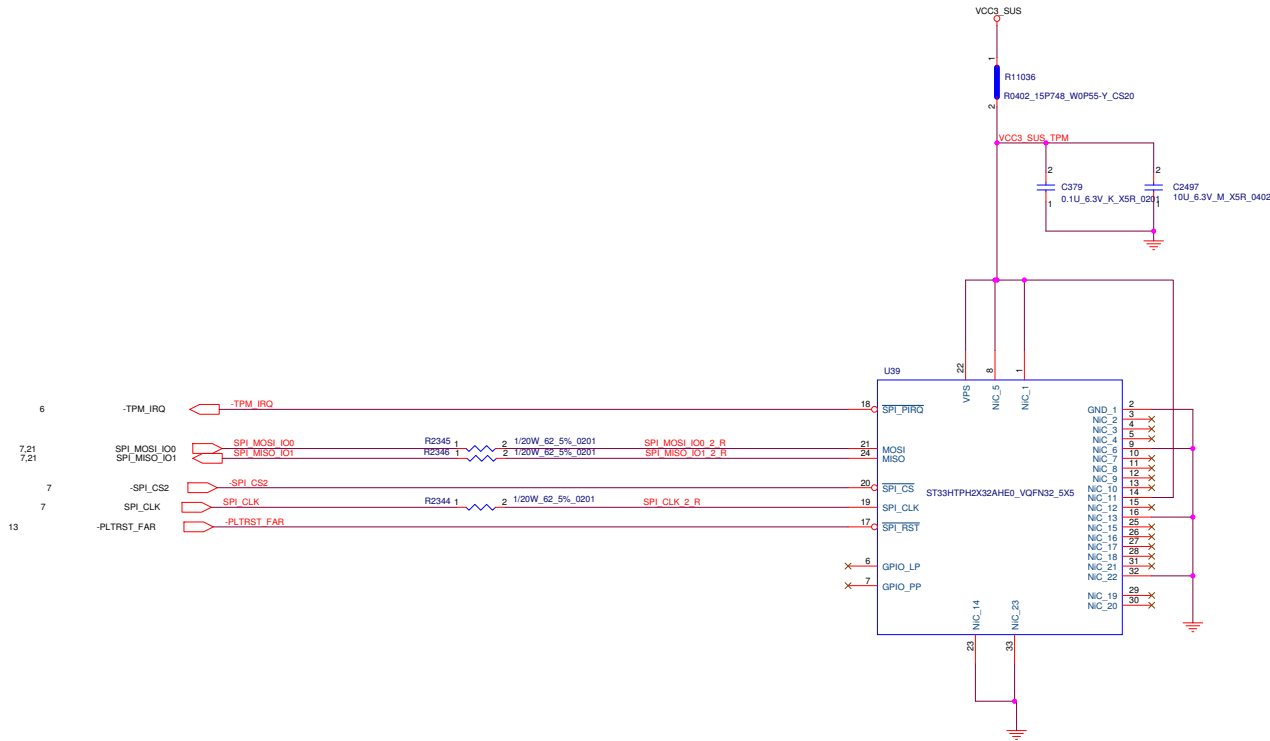


TABLE:J2101

WSON8 SPI FLASH SOCKET	
ACES	50950-0084N-001
DediProg	SOK-SPI-WSON68

TABLE:U49

64MB (512Mb) 8x6mm WSON	
Winbond	W25Q512JVEIN
GigaDevie	GD25B512MEYIGR
Macronix	MX25L51273GZ4I-08G



TABLE

Pin No	TCG PTP Spec Rev.01.03.v22	ST Micro ST33HTPH2X32AE0	Nuvoton NPCT760LAAYX	Infinion SLB 9672V2U2.0 FW15.21
1	VDD/VSB	NC	VSB	VDD
2	GND	GND	NC	GND
3	GPIO	NC	NC	GPIO_00
4	GPIO	NC	PP/GPIO6	GPIO_01
5	NC	NC	NC	NC
6	VNC/GPIO/I2C_PIRQ#	GPIO_LP	GPIO3	NC
7	GPIO/VDD	GPIO_PP	NC	GPIO_02
8	VDD	NC	VHIO	VDD
9	GND	NC	NC	GND
10	VNC	NC	NC	NC
11	NC	NC	NC	NC
12	NC	NC	NC	NC
13	VNC/GPIO/I2C_PIRQ#	NC	GPIO4	NC
14	VDD	NC	NC	VDD
15	NC	NC	NC	NC
16	GND	NC	GND	GND
17	SPI_RST#	SPI_RST#	PLTRST#	RST#
18	SPI_PIRQ#/I2C_PIRQ#	SPI_PIRQ#	PIRQ#/GPIO2	PIRQ#
19	SPI_CLK	SPI_CLK	SCLK	SCLK
20	SPI_CS#	SPI_CS#	SCS#/GPIO5	CS#
21	MOSI	MOSI	MOSI/GPIO7	MOSI
22	VDD	VPS	VHIO	VDD
23	GND	NC	GND	GND
24	MISO	MISO	MISO	MISO
25	NC	NC	NC	NC
26	NC	NC	NC	NC
27	VNC/GPIO	NC	NC	NC
28	VNC/GPIO	NC	NC	NC
29	SDA	NC	SDA/GPIO0	NC
30	SCL	NC	SCL/GPIO1	NC
31	VNC	NC	NC	NC
32	GND	NC	NC	GND

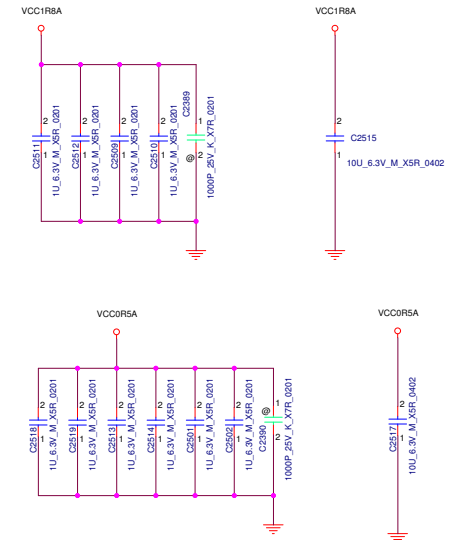
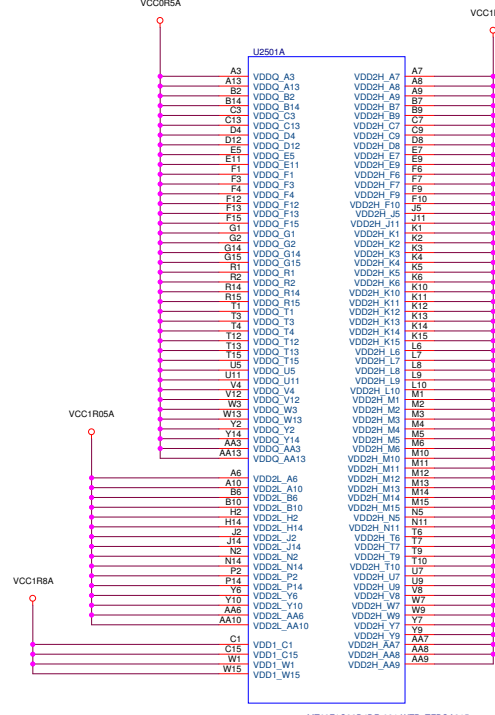
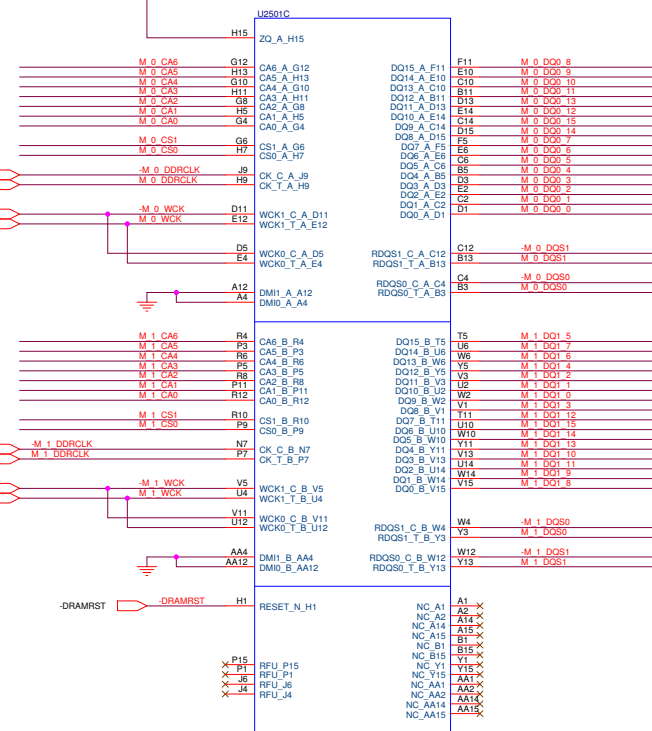
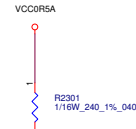
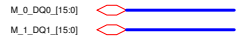


TABLE : LPDDR5 Source

Supplier	Capacity	Supplier's P/N	Package Size	Die	Device Configuration	Memory
SK hynix	16Gbit	H9JCNNNBK3MLYR-N6E	12.4 x 15 mm	DDP	8Gb die	1 Rank x (512Mx16) x 2 Ch
	32Gbit	H9JCNNNC3MLYR-N6E	12.4 x 15 mm	QDP	8Gb die	2 Rank x (512Mx16) x 2 Ch
	64Gbit	H9JCNNNFA5MLYR-N6E	12.4 x 15 mm	ODP	8Gb die	2 Rank x (1Gx16) x 2 Ch
Samsung	32Gbit	K3LKBK80BM-MGCP	12.4 x 15 mm	DDP	16Gb die	1 Rank x (1Gx16) x 2 Ch
	64Gbit	K3LKCCK0BM-MGCP	12.4 x 15 mm	QDP	16Gb die	2 Rank x (1Gx16) x 2 Ch
Micron	16Gbit	MT62F512M32D2DR-031 WT:B	12.4 x 15 mm	DDP	8Gb die	1 Rank x (512Mx16) x 2 Ch
	32Gbit	MT62F1G32D4DR-031 WT:B	12.4 x 15 mm	QDP	8Gb die	2 Rank x (512Mx16) x 2 Ch
	64Gbit	MT62F2G32D8DR-031 WT:B	12.4 x 15 mm	ODP	8Gb die	2 Rank x (1Gx16) x 2 Ch



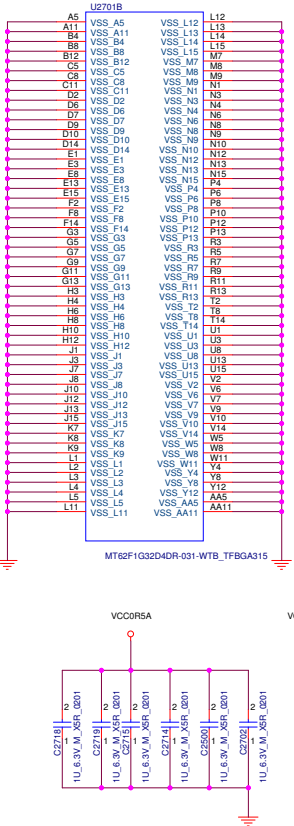
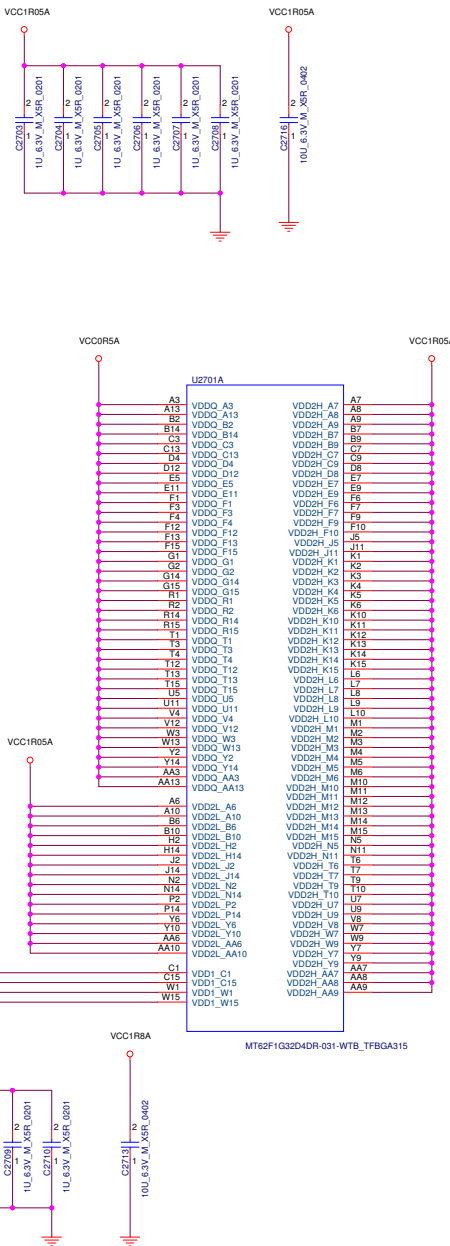
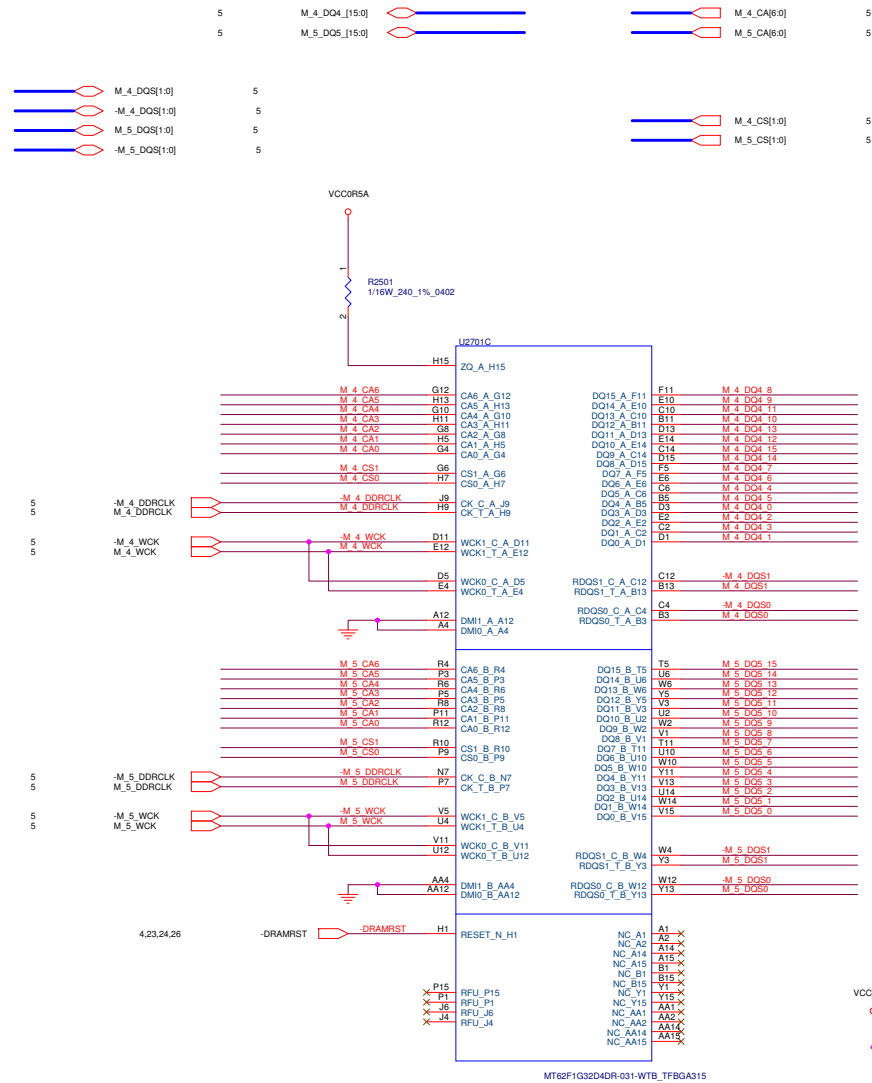
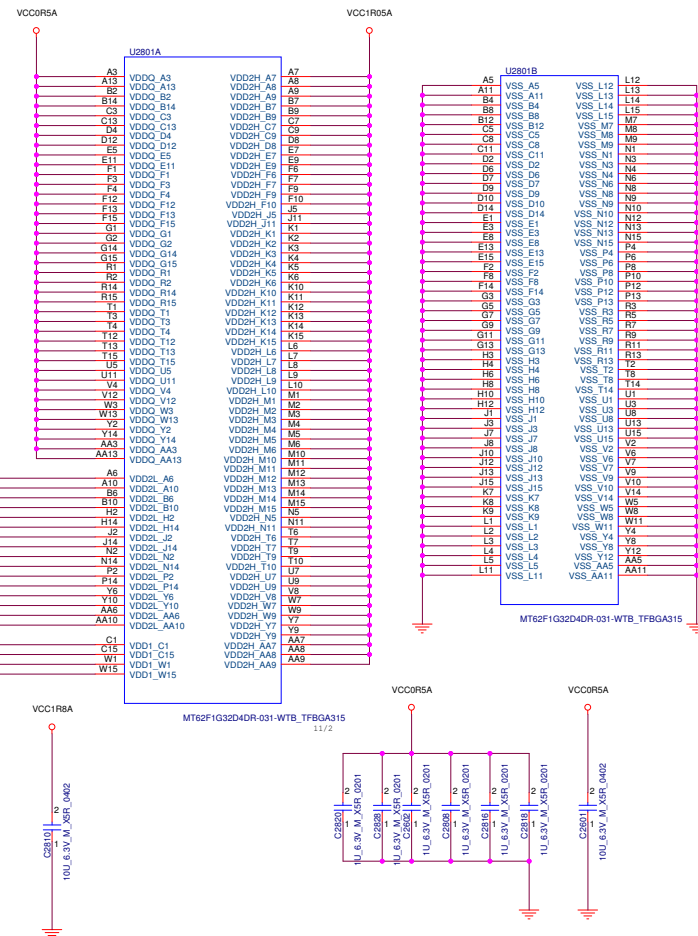
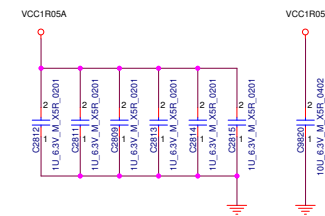


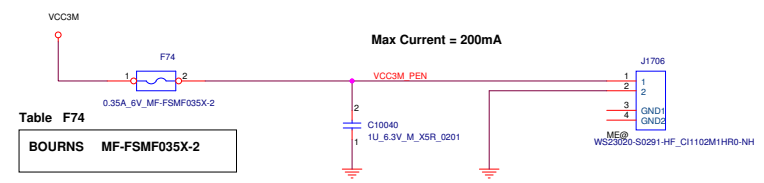
TABLE : LPDDR5 Source							
Supplier	Capacity	Supplier's P/N	Package Size		Die	Device Configuration	Memory
SK hynix	16Gbit	H9JCNNNBK3MLYR-N6E	12.4 x 15 mm	DDP	8Gb die	1 Rank x (512Mx16) x 2 Ch	8GB
	32Gbit	H9JCNNNCP3MLYR-N6E	12.4 x 15 mm	QDP	8Gb die	2 Rank x (512Mx16) x 2 Ch	16GB
	64Gbit	H9JCNNNFA5MLYR-N6E	12.4 x 15 mm	ODP	8Gb die	2 Rank x (1Gx16) x 2 Ch	32GB
Samsung	32Gbit	K3LKBK80BM-MGCP	12.4 x 15 mm	DDP	16Gb die	1 Rank x (1Gx16) x 2 Ch	16GB
	64Gbit	K3LKBK80BM-MGCP	12.4 x 15 mm	QDP	16Gb die	2 Rank x (1Gx16) x 2 Ch	32GB
Micron	16Gbit	MT62F512M32D2DR-031 WT:B	12.4 x 15 mm	DDP	8Gb die	1 Rank x (512Mx16) x 2 Ch	8GB
	32Gbit	MT62F1G32D4DR-031 WT:B	12.4 x 15 mm	QDP	8Gb die	2 Rank x (512Mx16) x 2 Ch	16GB
	64Gbit	MT62F2G32D8DR-031 WT:B	12.4 x 15 mm	ODP	8Gb die	2 Rank x (1Gx16) x 2 Ch	32GB



Supplier	Capacity	Supplier's P/N	Package Size		Die	Device Configuration	Memory
SK hynix	16Gbit	H9JCNNNBK3MLYR-N6E	12.4 x 15 mm	DDP	8Gb die	1 Rank x (512Mx16) x 2 Ch	8GB
	32Gbit	H9JCNNNCP3MLYR-N6E	12.4 x 15 mm	QDP	8Gb die	2 Rank x (512Mx16) x 2 Ch	16GB
	64Gbit	H9JCNNNFA5MLYR-N6E	12.4 x 15 mm	ODP	8Gb die	2 Rank x (1Gx16) x 2 Ch	32GB
Samsung	32Gbit	K3LK8KB08M-MGCP	12.4 x 15 mm	DDP	16Gb die	1 Rank x (1Gx16) x 2 Ch	16GB
	64Gbit	K3LKCKC08M-MGCP	12.4 x 15 mm	QDP	16Gb die	2 Rank x (1Gx16) x 2 Ch	32GB
Micron	16Gbit	MT62F512M32D2DR-031 WT:B	12.4 x 15 mm	DDP	8Gb die	1 Rank x (512Mx16) x 2 Ch	8GB
	32Gbit	MT62F1G32D4DR-031 WT:B	12.4 x 15 mm	QDP	8Gb die	2 Rank x (512Mx16) x 2 Ch	16GB
	64Gbit	MT62F2G32D8DR-031 WT:B	12.4 x 15 mm	ODP	8Gb die	2 Rank x (1Gx16) x 2 Ch	32GB

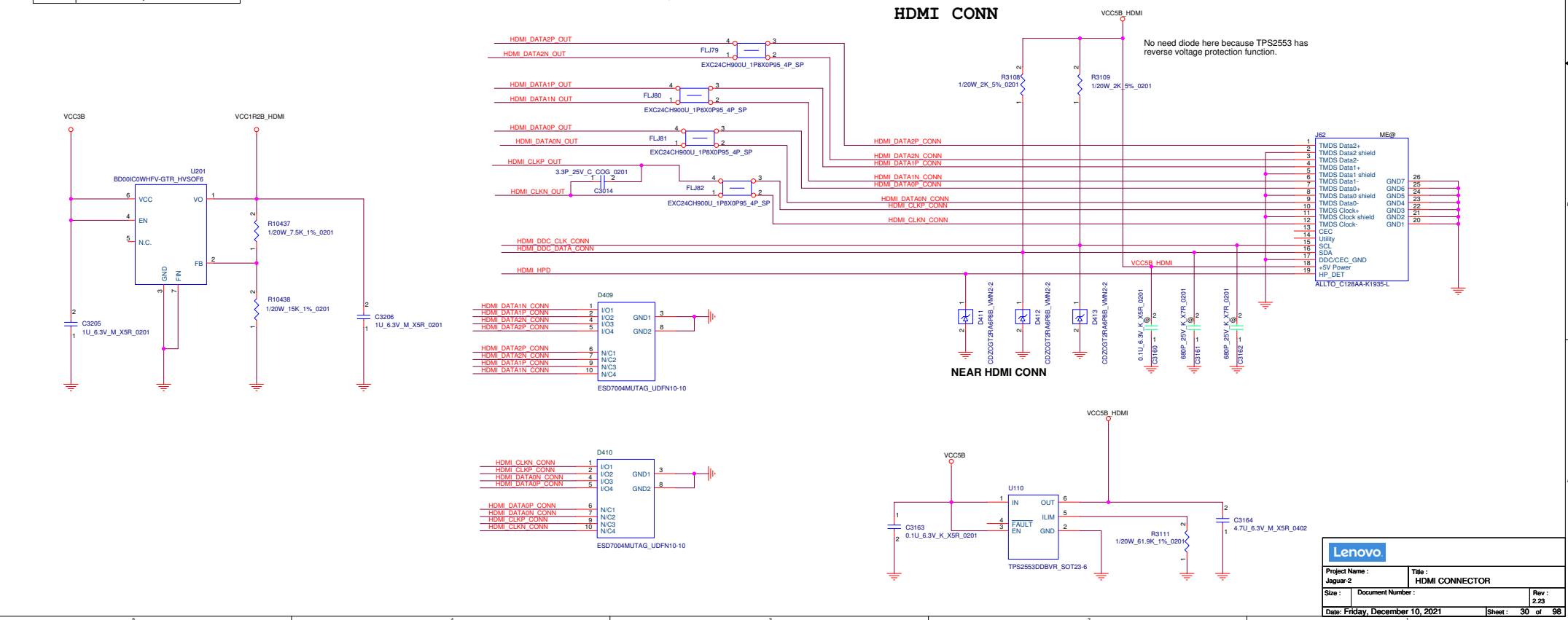
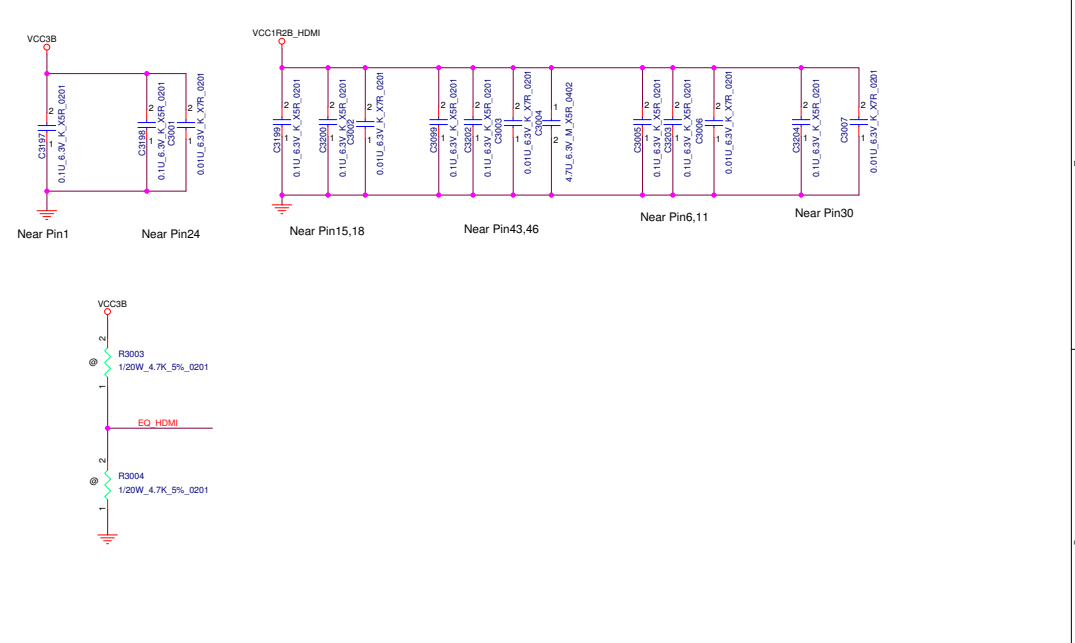
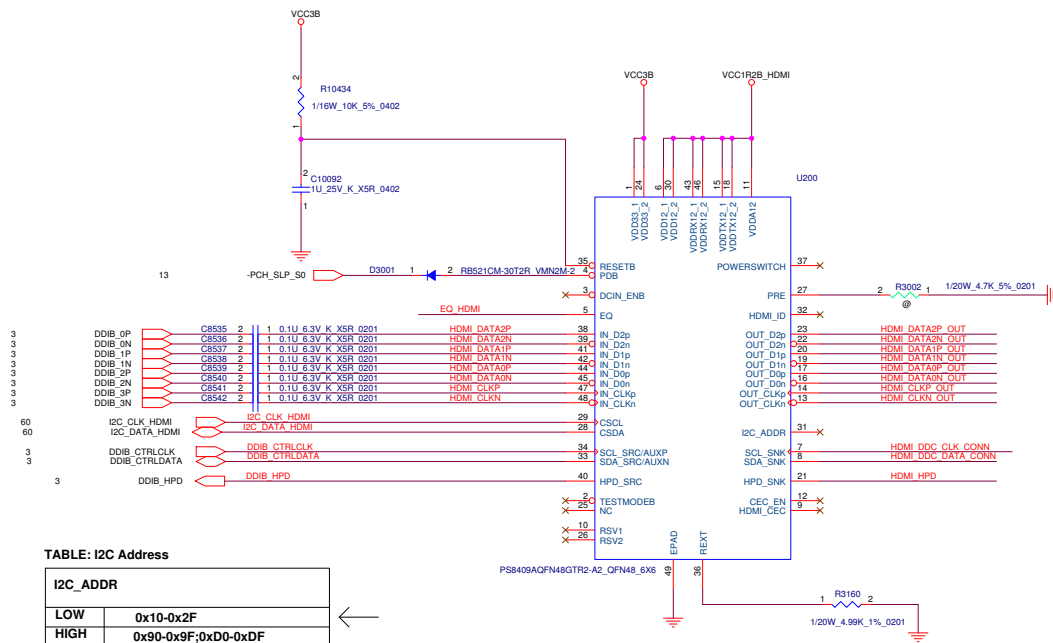






**Table F74**

BOURNS	MF-FSMF035X-2
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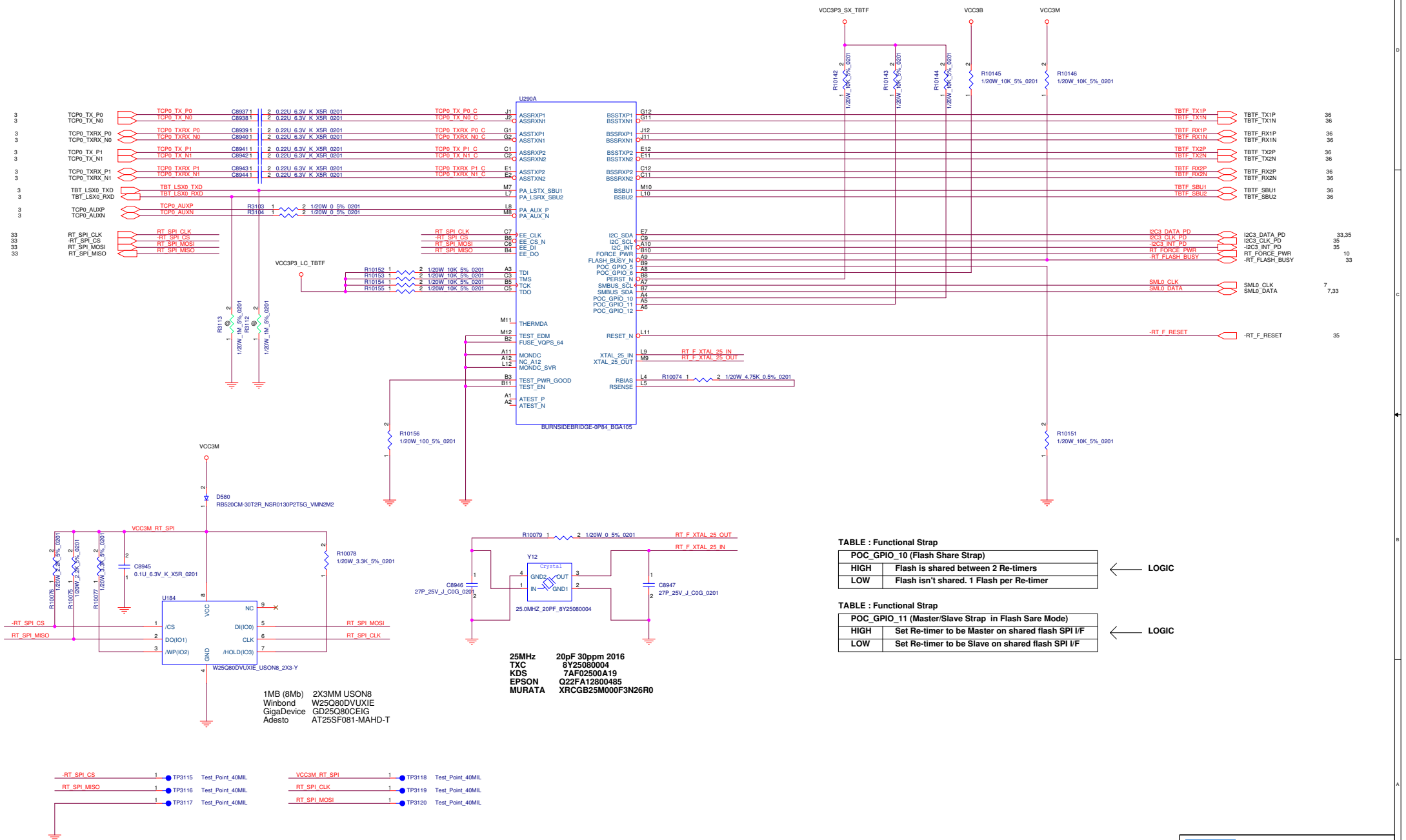


TABLE : Functional Strap

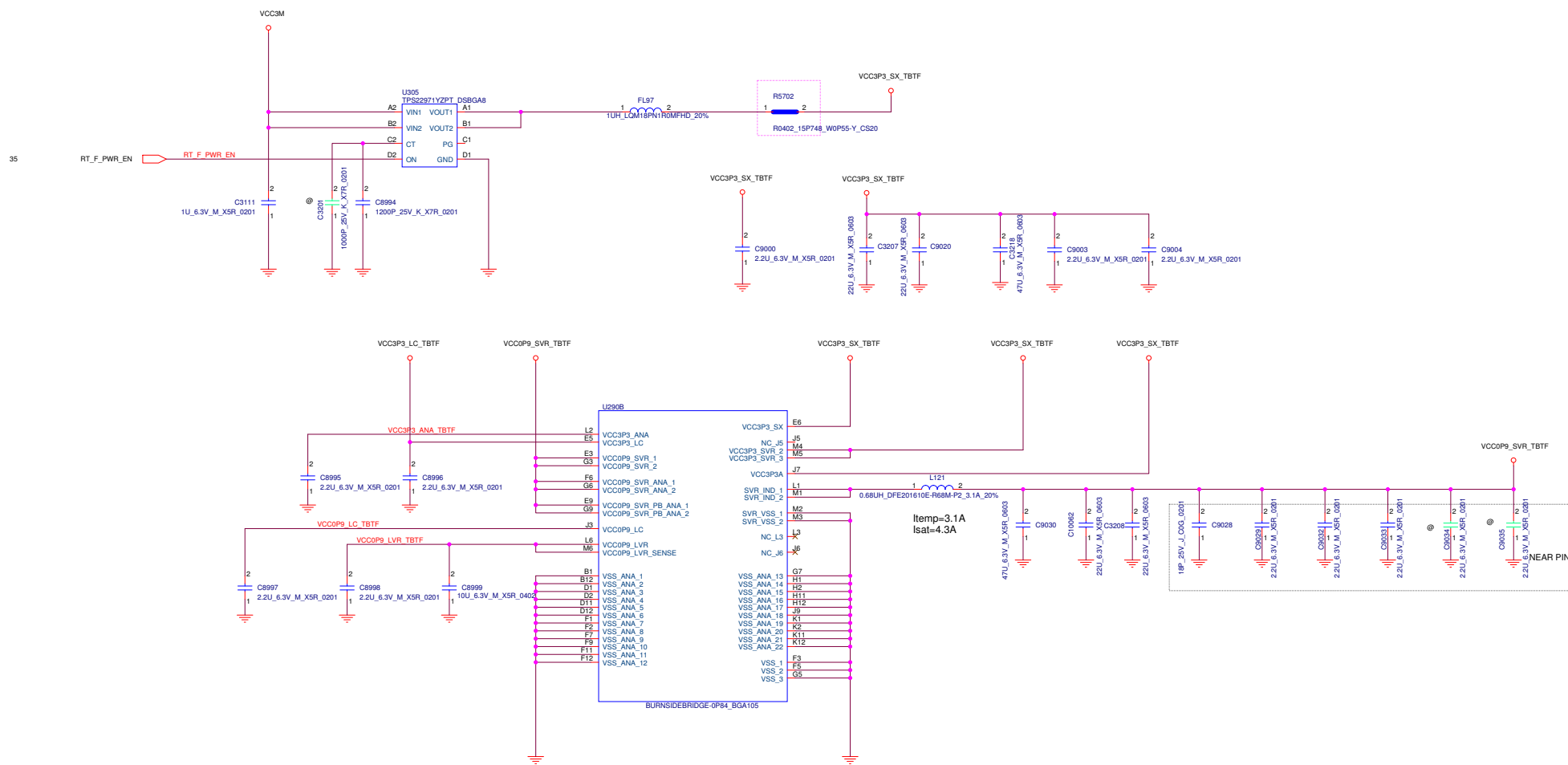
POC_GPIO_10 (Flash Share Strap)	
HIGH	Flash is shared between 2 Re-timers
LOW	Flash isn't shared. 1 Flash per Re-timer

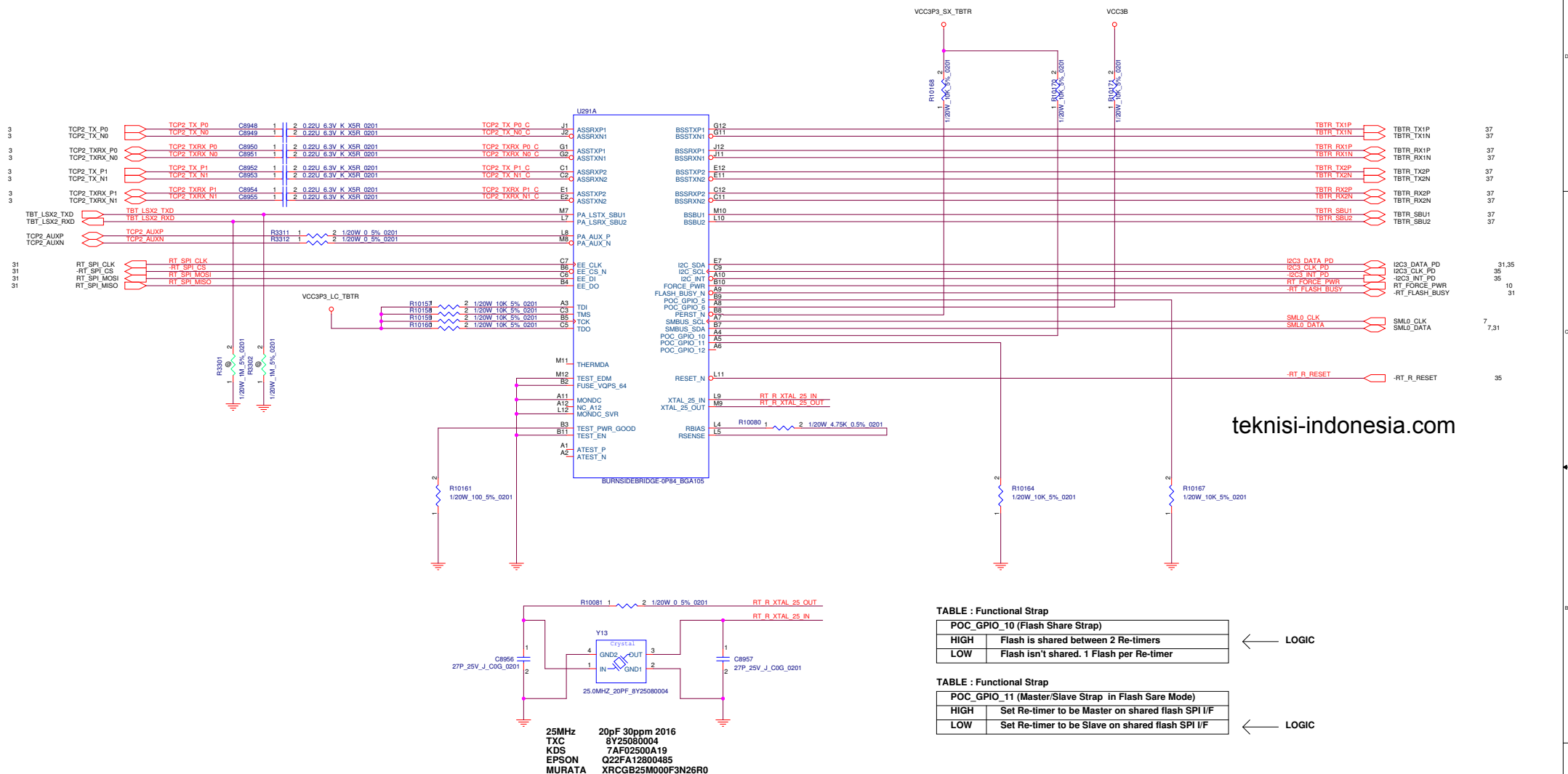
← LOGIC

TABLE : Functional Strap

POC_GPIO_11 (Master/Slave Strap in Flash Sare Mode)	
HIGH	Set Re-timer to be Master on shared flash SPI I/F
LOW	Set Re-timer to be Slave on shared flash SPI I/F

← LOGIC





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TABLE : Functional Strap

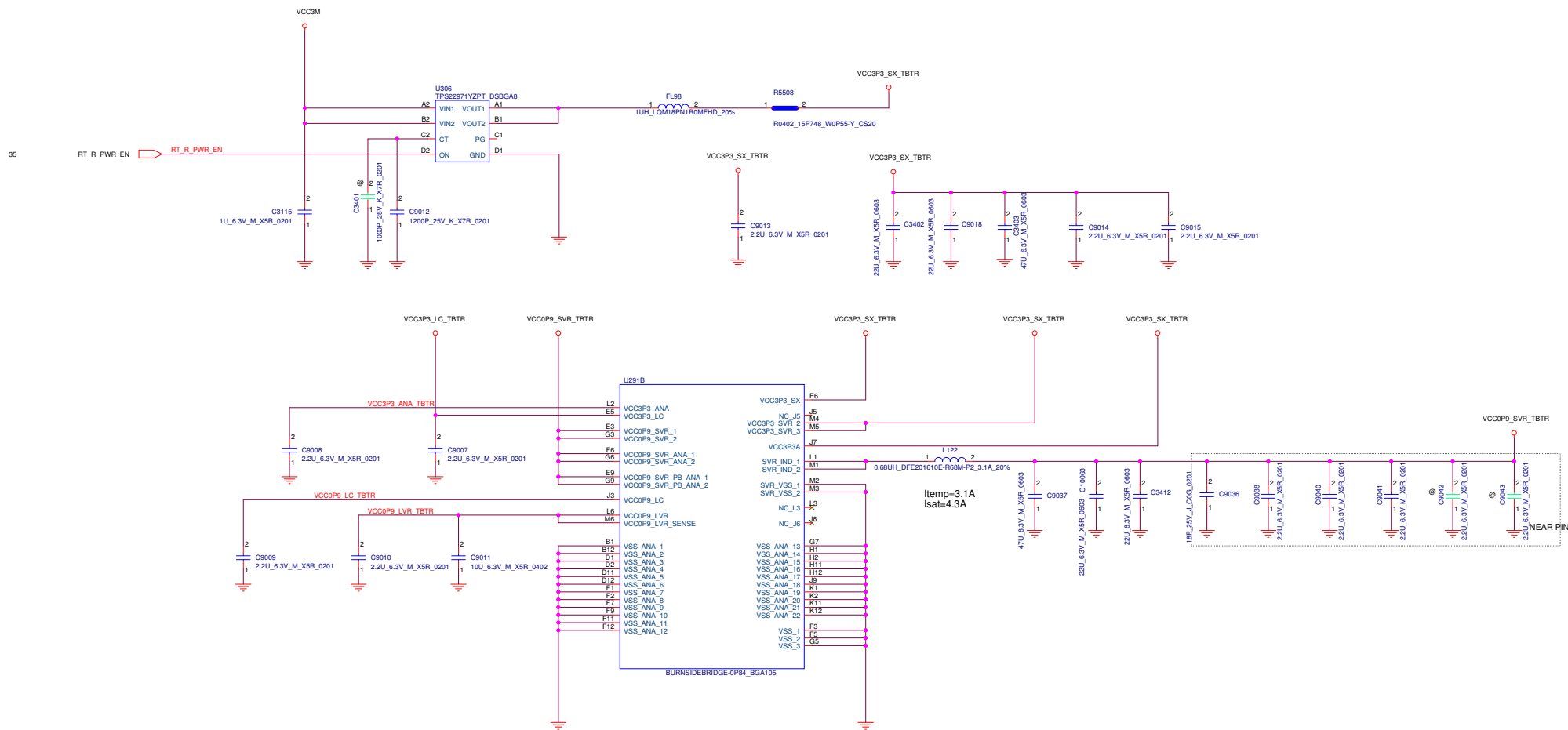
POC_GPIO_10 (Flash Share Strap)	
HIGH	Flash is shared between 2 Re-timers
LOW	Flash isn't shared. 1 Flash per Re-timer

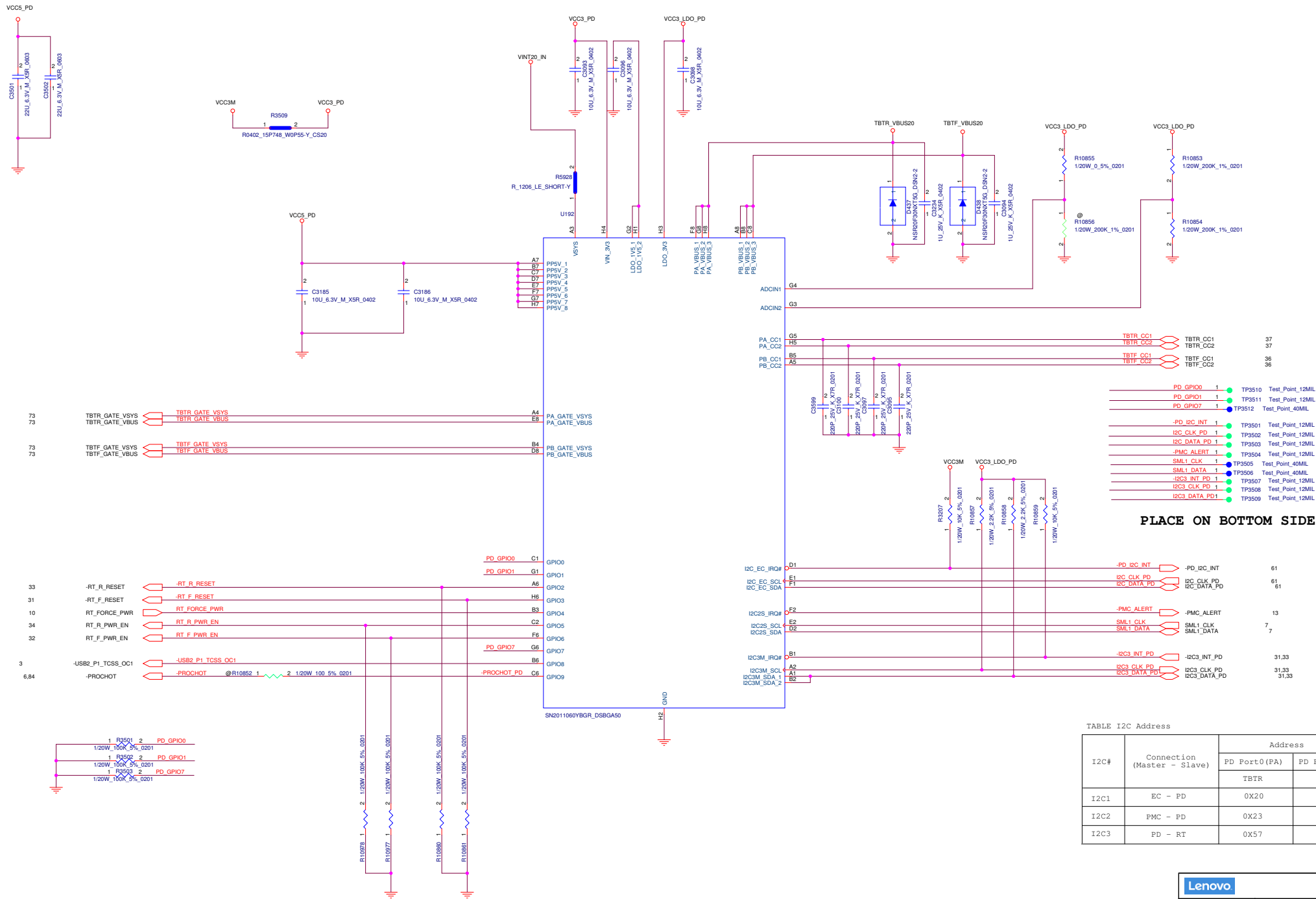
← LOGIC

TABLE : Functional Strap

POC_GPIO_11 (Master/Slave Strap in Flash Sare Mode)	
HIGH	Set Re-timer to be Master on shared flash SPI I/F
LOW	Set Re-timer to be Slave on shared flash SPI I/F

← LOGIC





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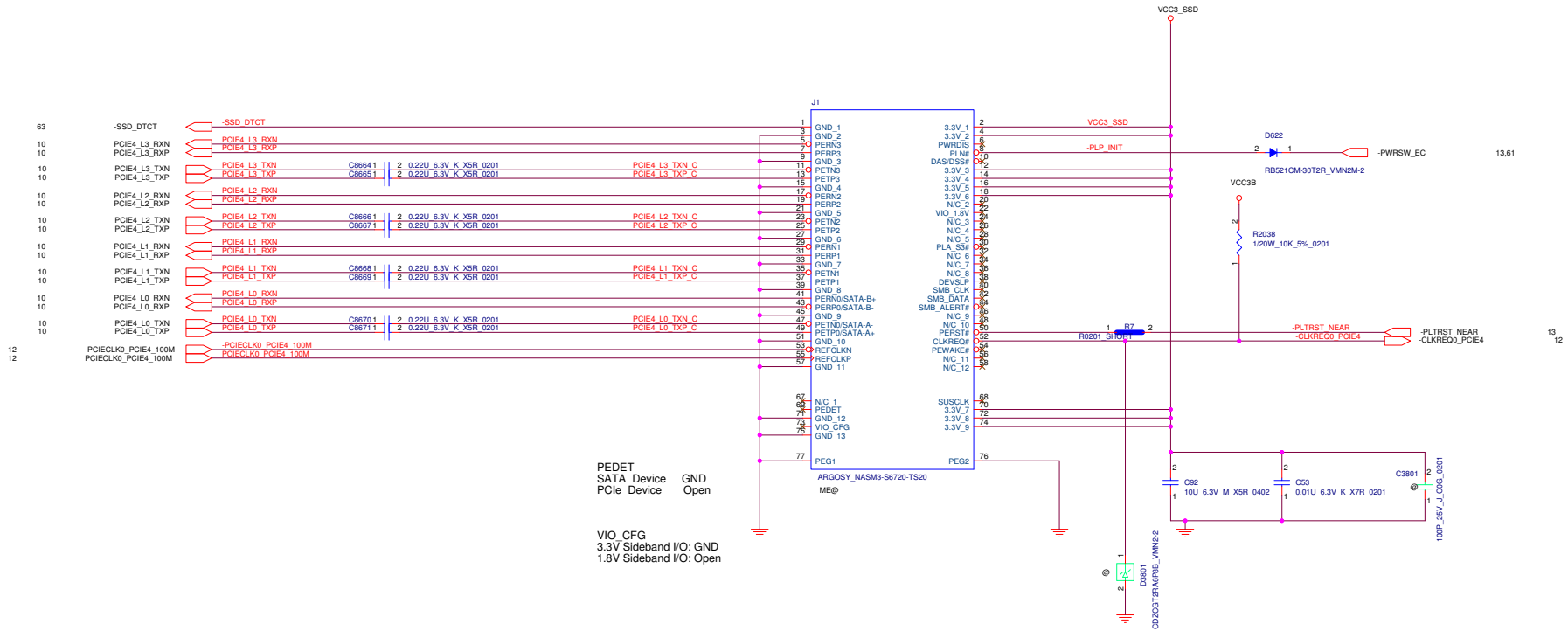
Project Name : Jaguar-2  
 Title : USB PD CONTROLLER  
 Size : Document Number :  
 Date : Friday, December 10, 2021  
 Rev : 2.23  
 Sheet : 35 of 98



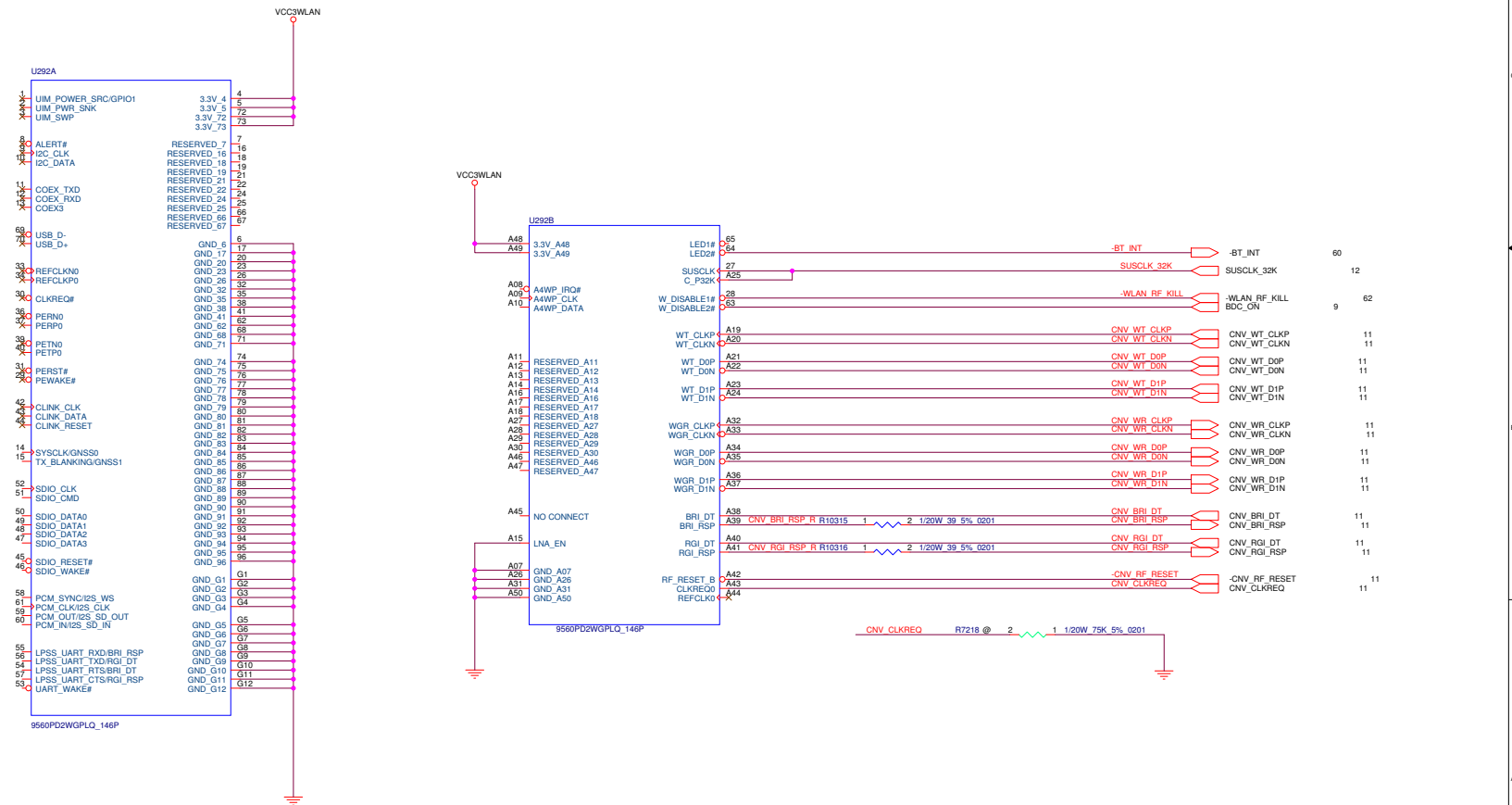


## M.2 Socket 3 (Key-M) for 2280 S3 SSD

H=2.00mm Connector



## M.2 Type 1216 Module for WLAN / Bluetooth



# M.2 Socket 2 (Key-B) for WWAN 3G/4G: 3042 S3 5G: 3042 S3 or 3052 S3 H=2.00mm Connector

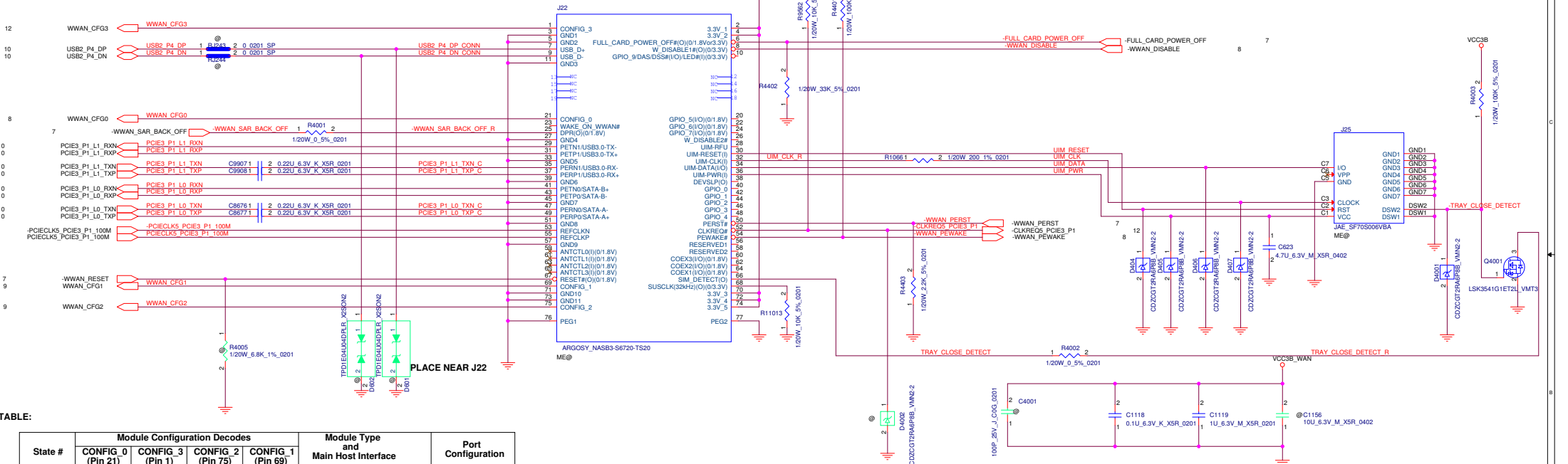
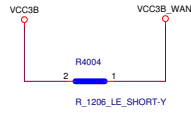
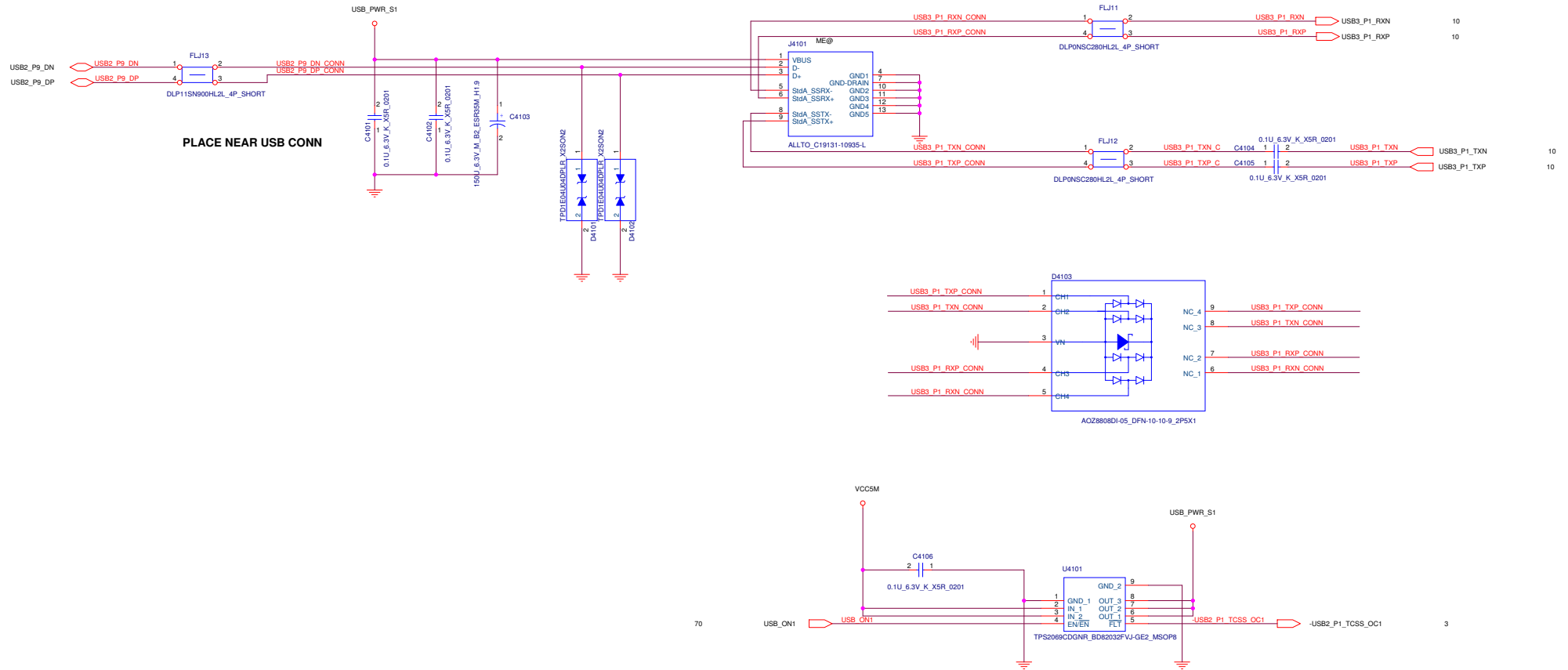
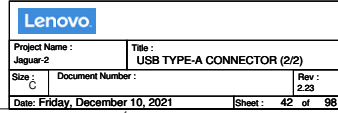


TABLE:

State #	Module Configuration Decodes				Module Type and Main Host Interface	Port Configuration
	CONFIG 0 (Pin 21)	CONFIG 3 (Pin 1)	CONFIG 2 (Pin 75)	CONFIG 1 (Pin 69)		
0	GND	GND	GND	GND	SSD - SATA	N/A
1	GND	GND	GND	NC	SSD - PCIe	N/A
2	GND	GND	NC	GND	WWAN - PCIe	0
3	GND	GND	NC	NC	WWAN - PCIe	1
4	GND	NC	GND	GND	WWAN - PCIe, USB 3.1 Gen1	0
5	GND	NC	GND	NC	WWAN - PCIe, USB 3.1 Gen1	1
6	GND	NC	NC	GND	WWAN - PCIe, USB 3.1 Gen1	2
7	GND	NC	NC	NC	WWAN - PCIe, USB 3.1 Gen1	3
8	NC	GND	GND	GND	WWAN - SSIC	0
9	NC	GND	GND	NC	WWAN - SSIC	1
10	NC	GND	NC	GND	WWAN - SSIC	2
11	NC	GND	NC	NC	WWAN - SSIC	3
12	NC	NC	GND	GND	WWAN - PCIe	2
13	NC	NC	GND	NC	WWAN - PCIe	3
14	NC	NC	NC	GND	WWAN - PCIe, USB 3.1 Gen1	Vendor Defined
15	NC	NC	NC	NC	No Module Present	N/A













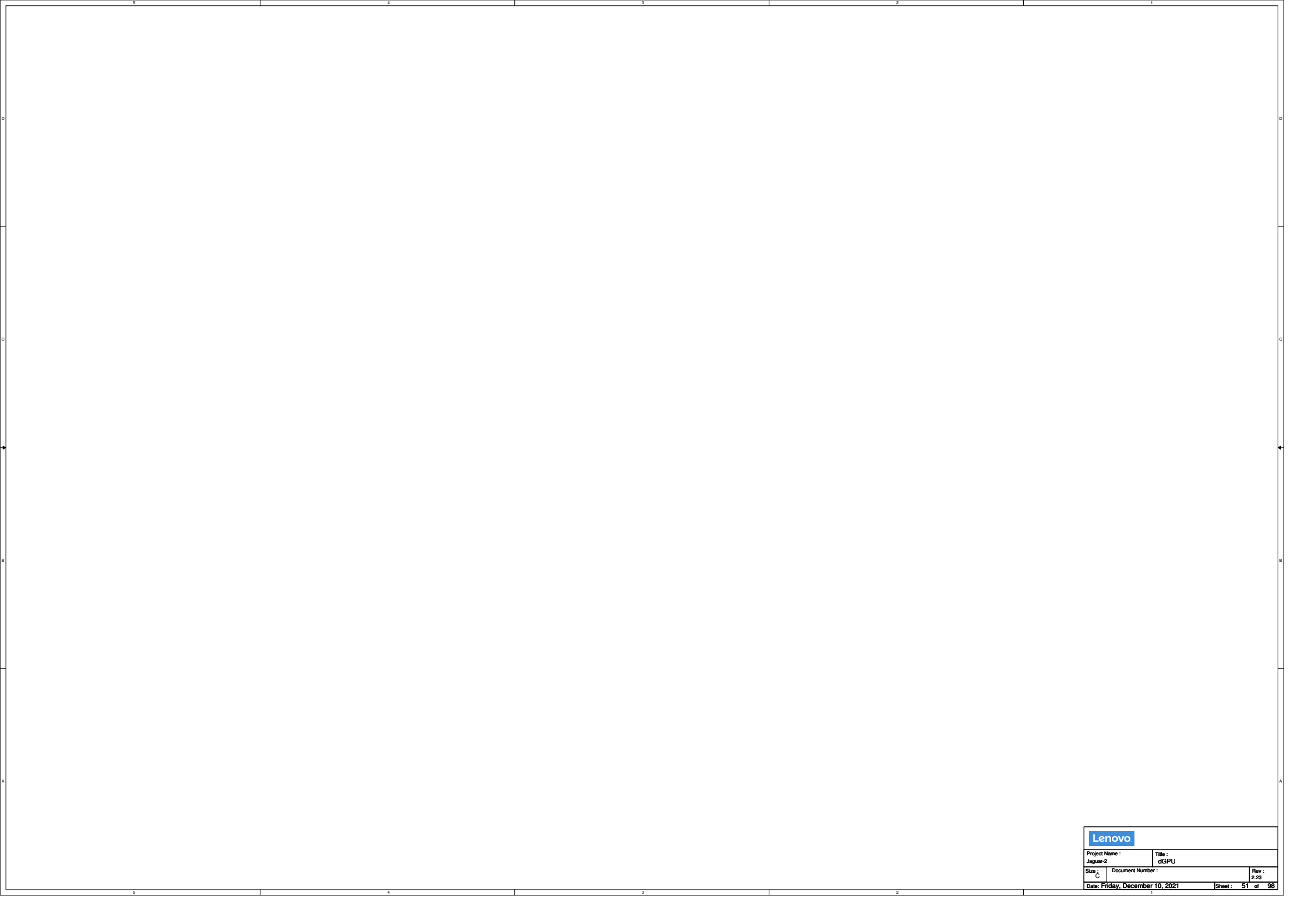
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<div>Lenovo</div>		
Project Name : Jaguar-2		Title : Media Card Slot
Size : C	Document Number :	Rev : 2.29
Date: Friday, December 10, 2021		Sheet : 47 of 98









Lenovo

Project Name :

Jaguar-2

Title :

dGPU

Size :

C

Document Number :

Rev :

2.29

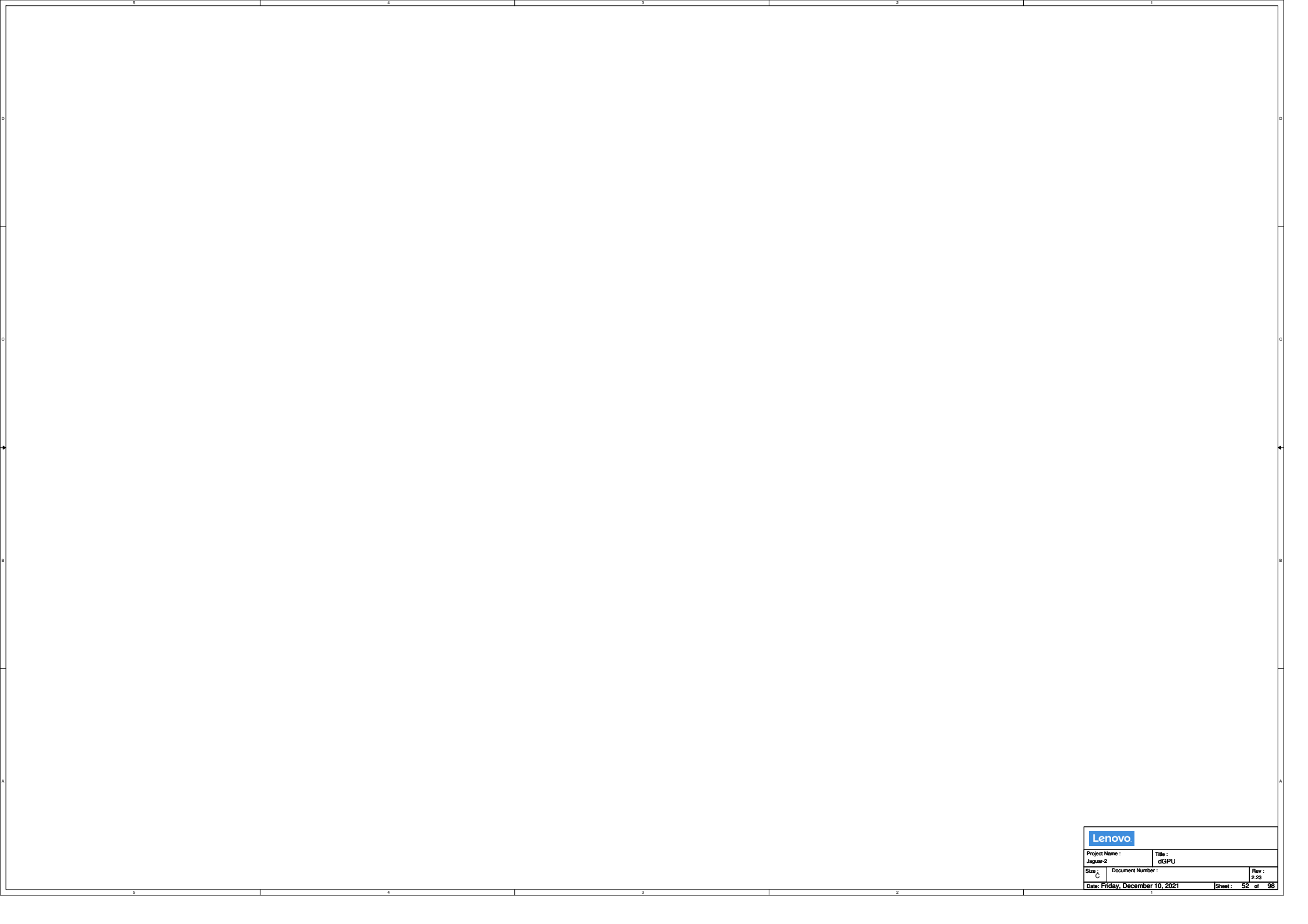
Date: Friday, December 10, 2021

Sheet :

51

of

98



Lenovo

Project Name :

Jaguar-2

Title :

dGPU

Size :

C

Document Number :

Rev :

2.29

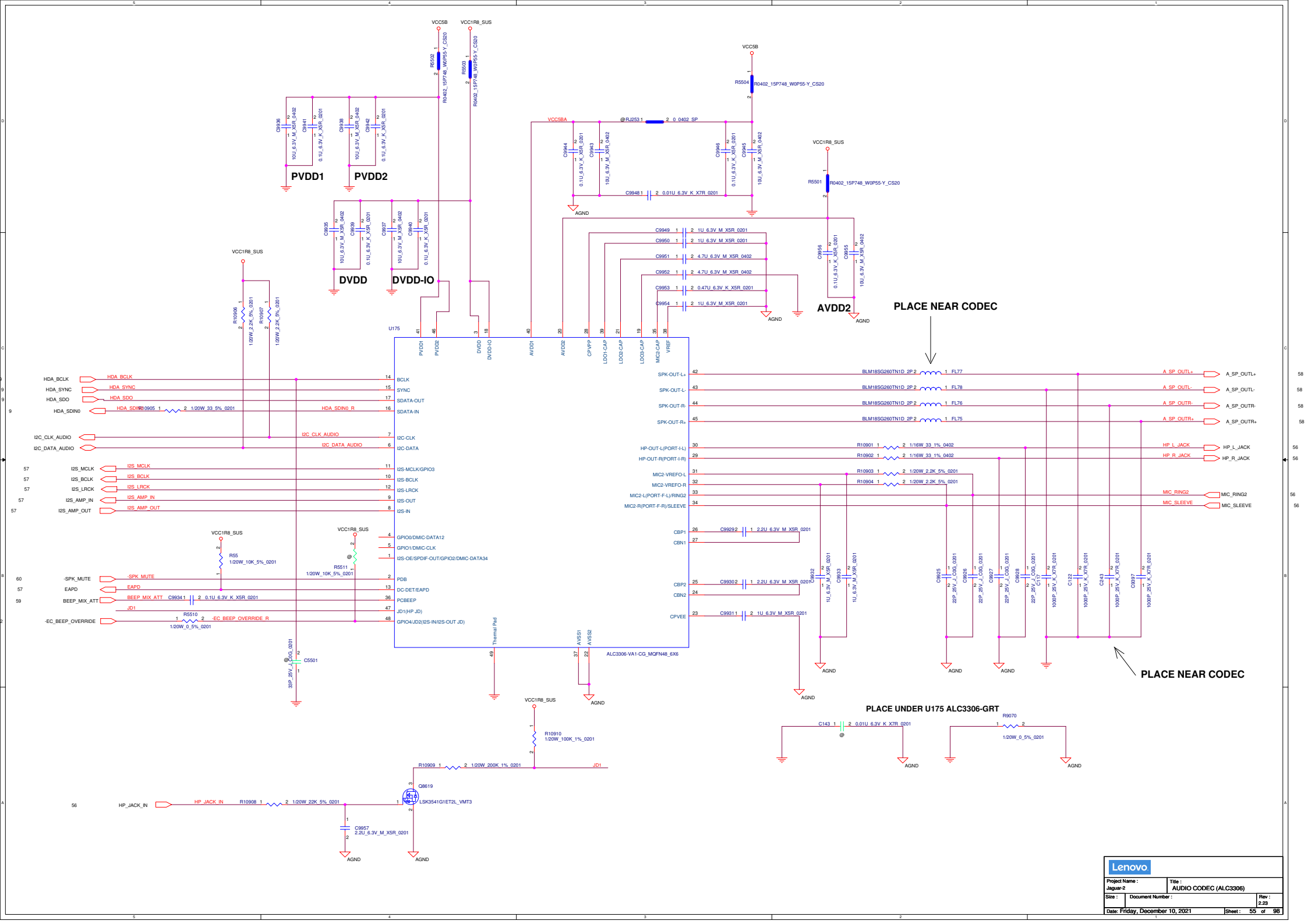
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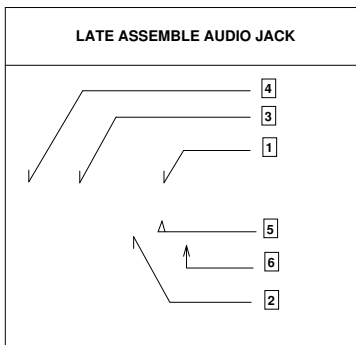
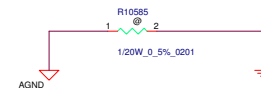
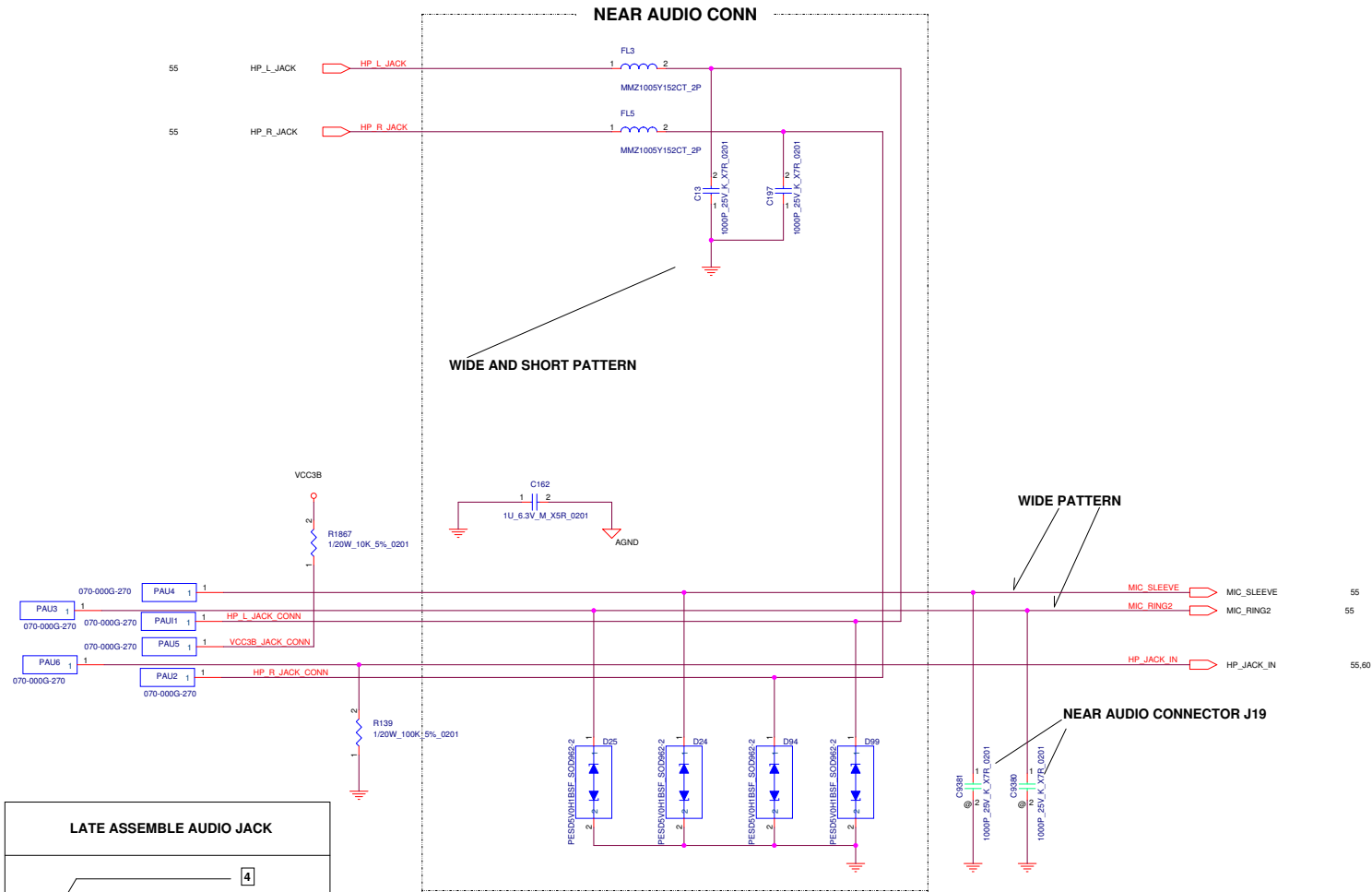
Sheet :

52 of 98



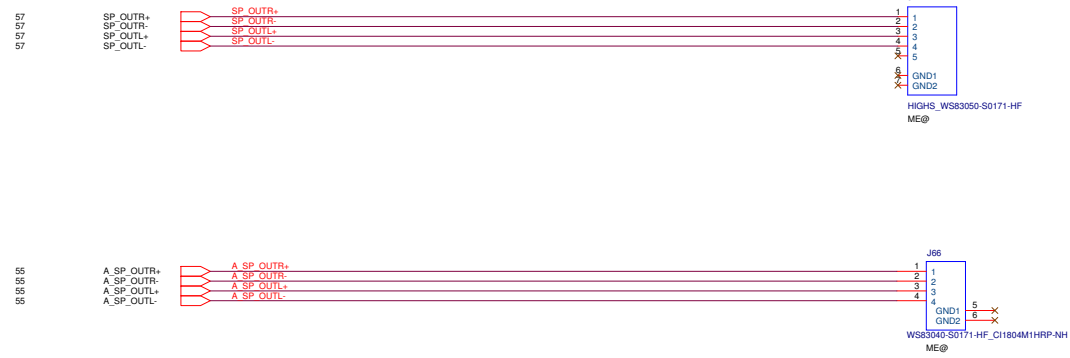


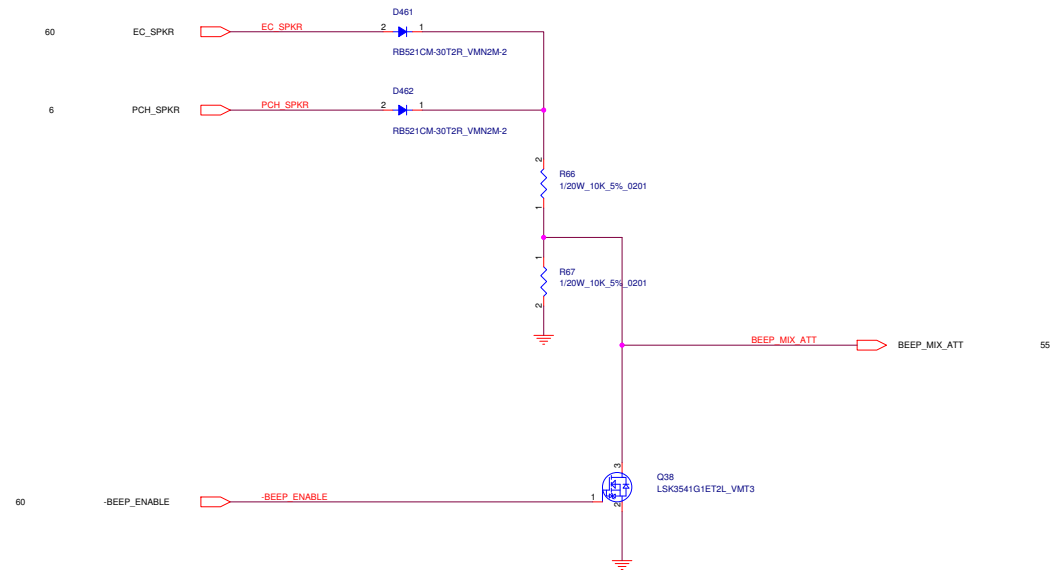




Pin 5 and 6 : Normal Open







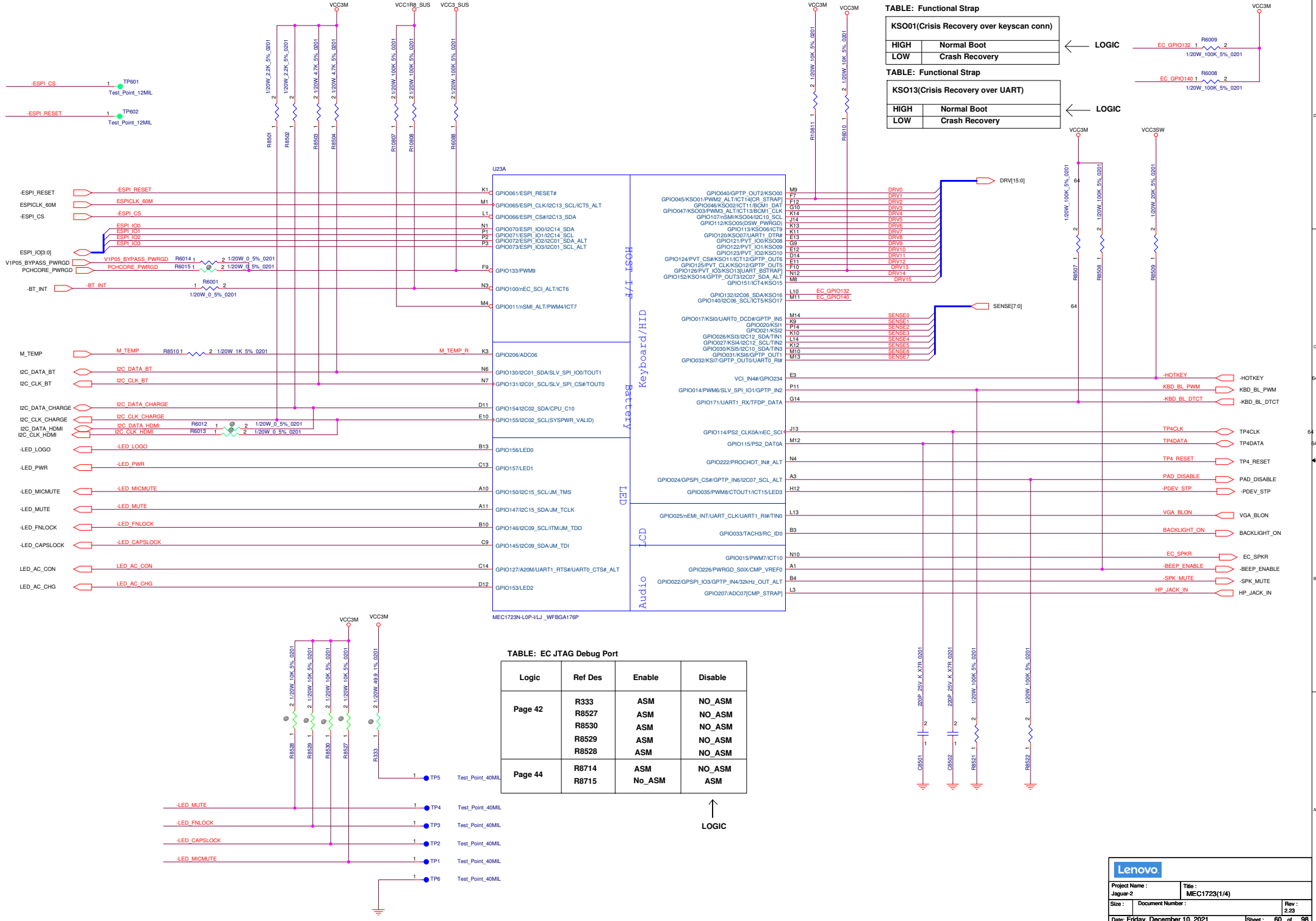


TABLE: Functional Strap

KSO01(Crisis Recovery over keyscan conn)	
HIGH	Normal Boot
LOW	Crash Recovery

LOGIC

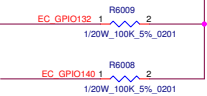


TABLE: Functional Strap

KSO13(Crisis Recovery over UART)	
HIGH	Normal Boot
LOW	Crash Recovery

LOGIC

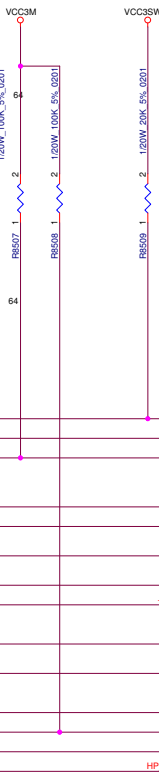
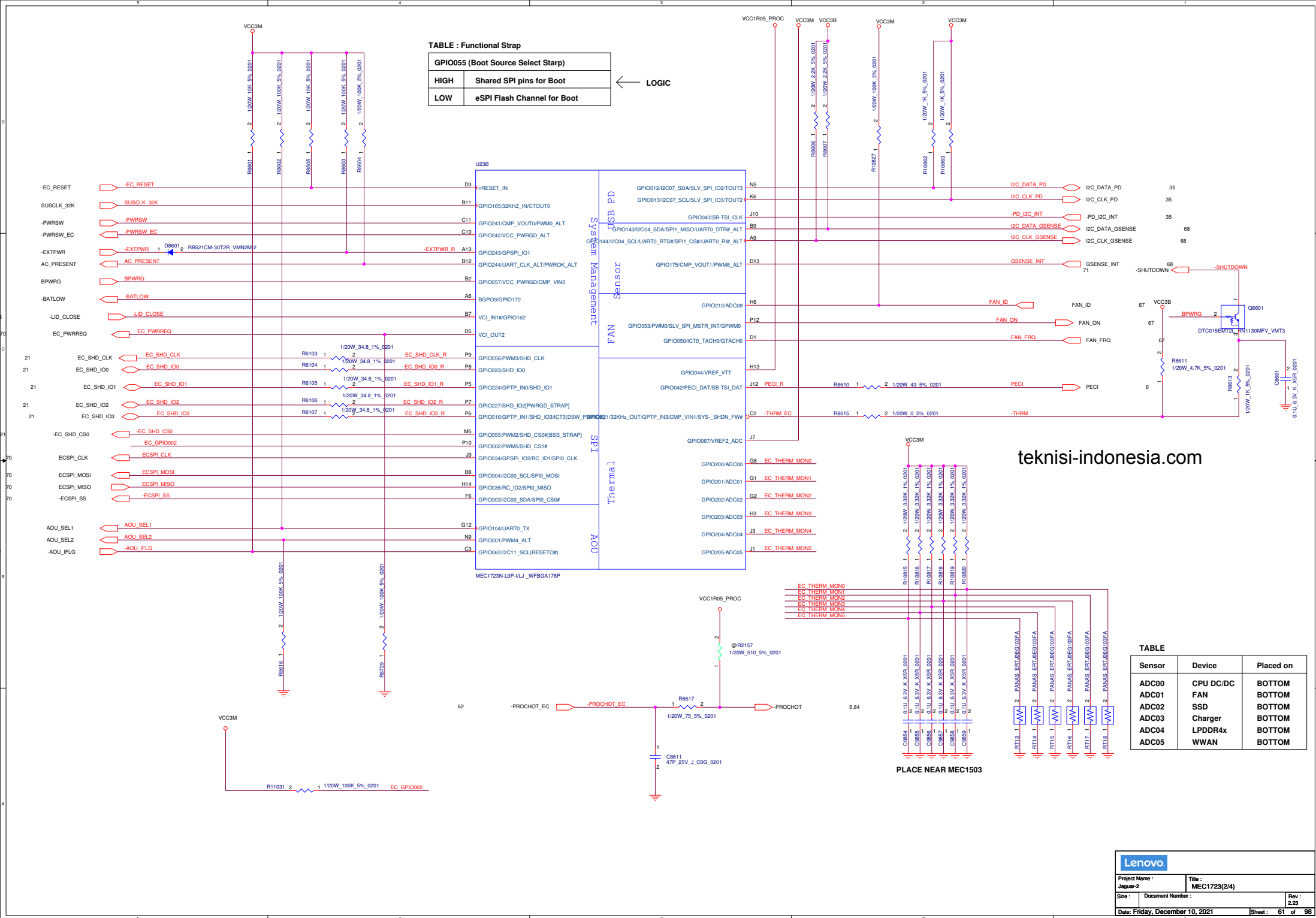


TABLE: EC JTAG Debug Port

Logic	Ref Des	Enable	Disable
Page 42	R333	ASM	NO_ASM
	R8527	ASM	NO_ASM
	R8530	ASM	NO_ASM
	R8529	ASM	NO_ASM
	R8528	ASM	NO_ASM
Page 44	R8714	ASM	NO_ASM
	R8715	No_ASM	ASM

LOGIC



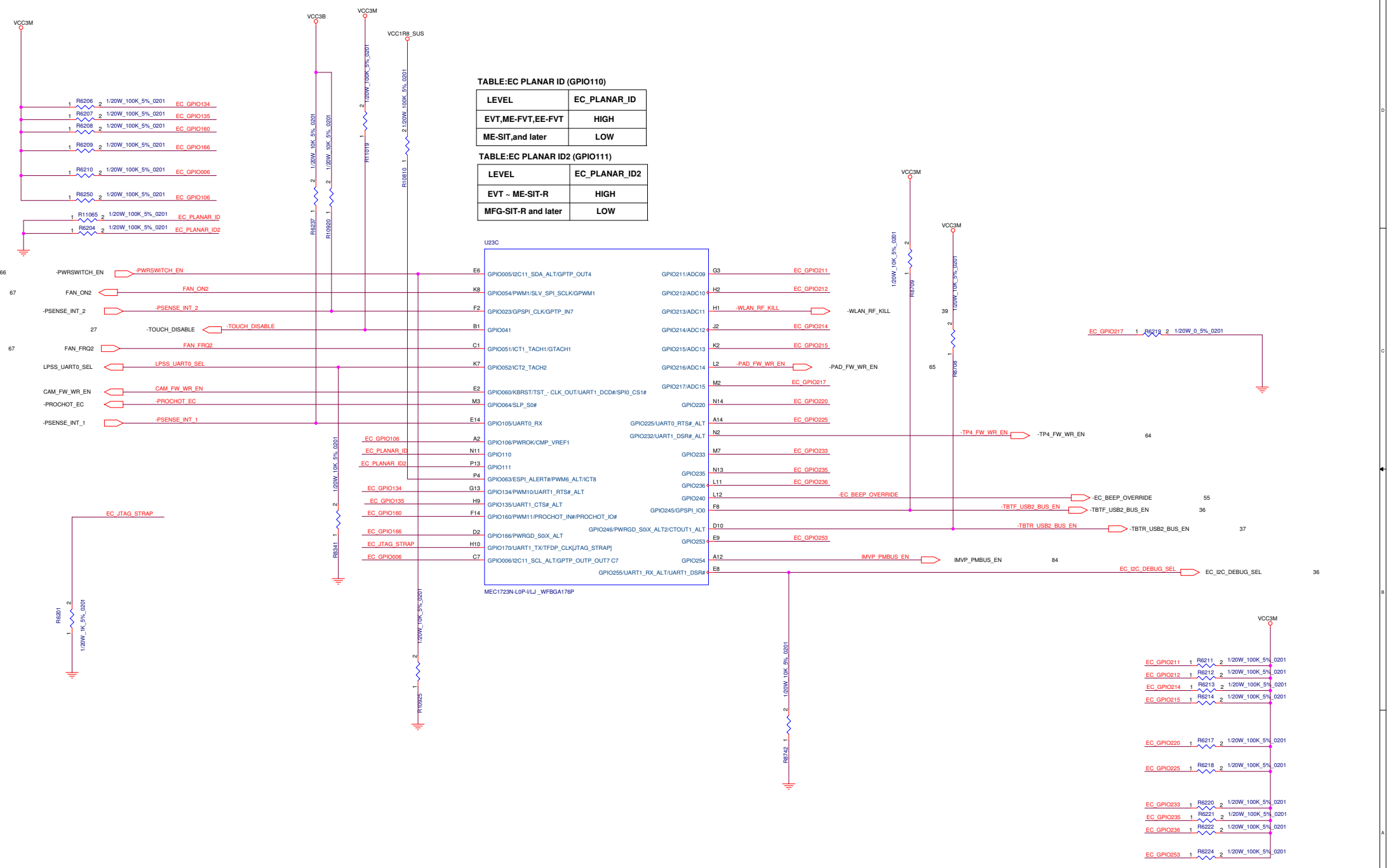


TABLE:EC PLANAR ID (GPIO110)

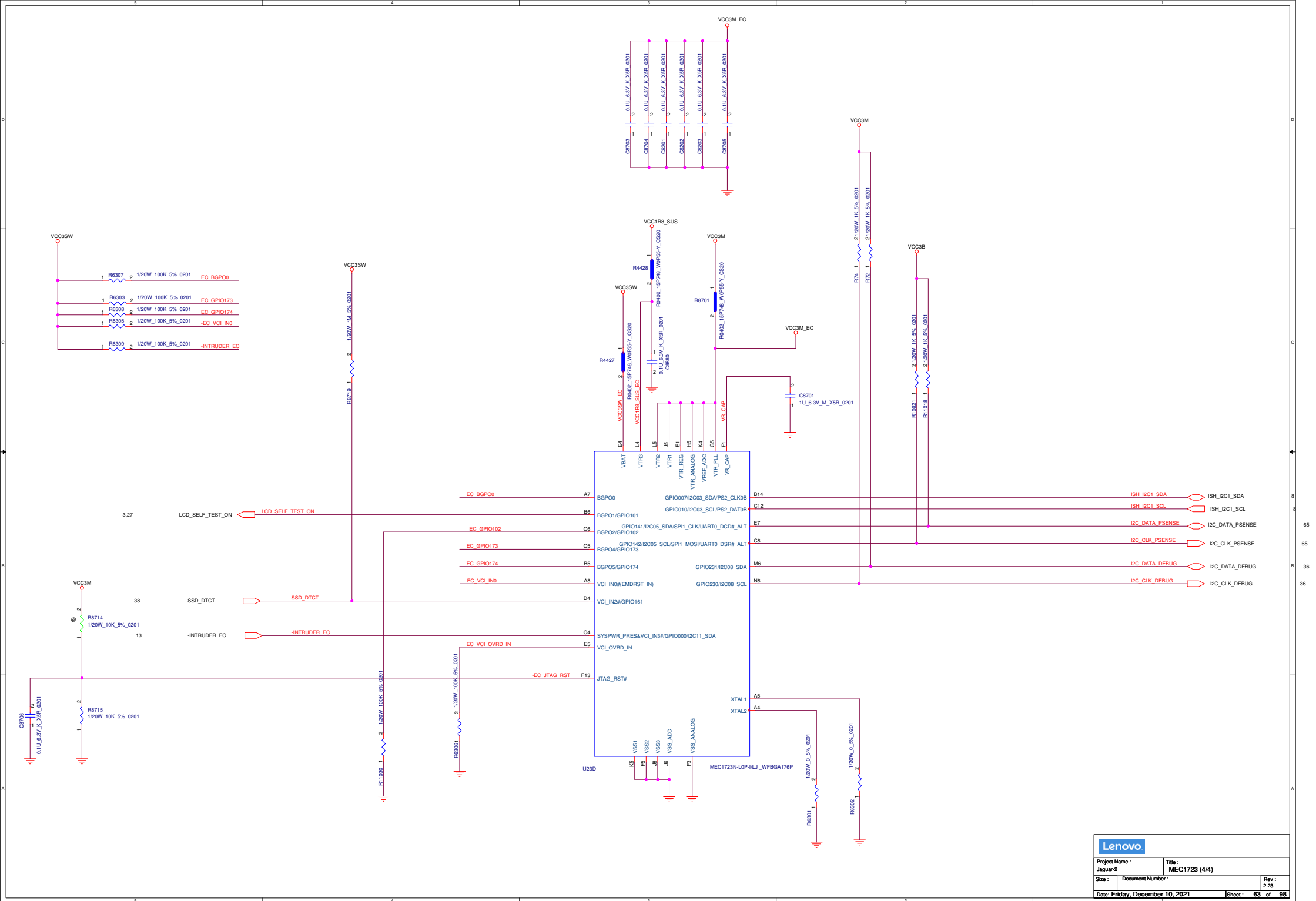
LEVEL	EC_PLANAR_ID
EVT,ME-FVT,EE-FVT	HIGH
ME-SIT,and later	LOW

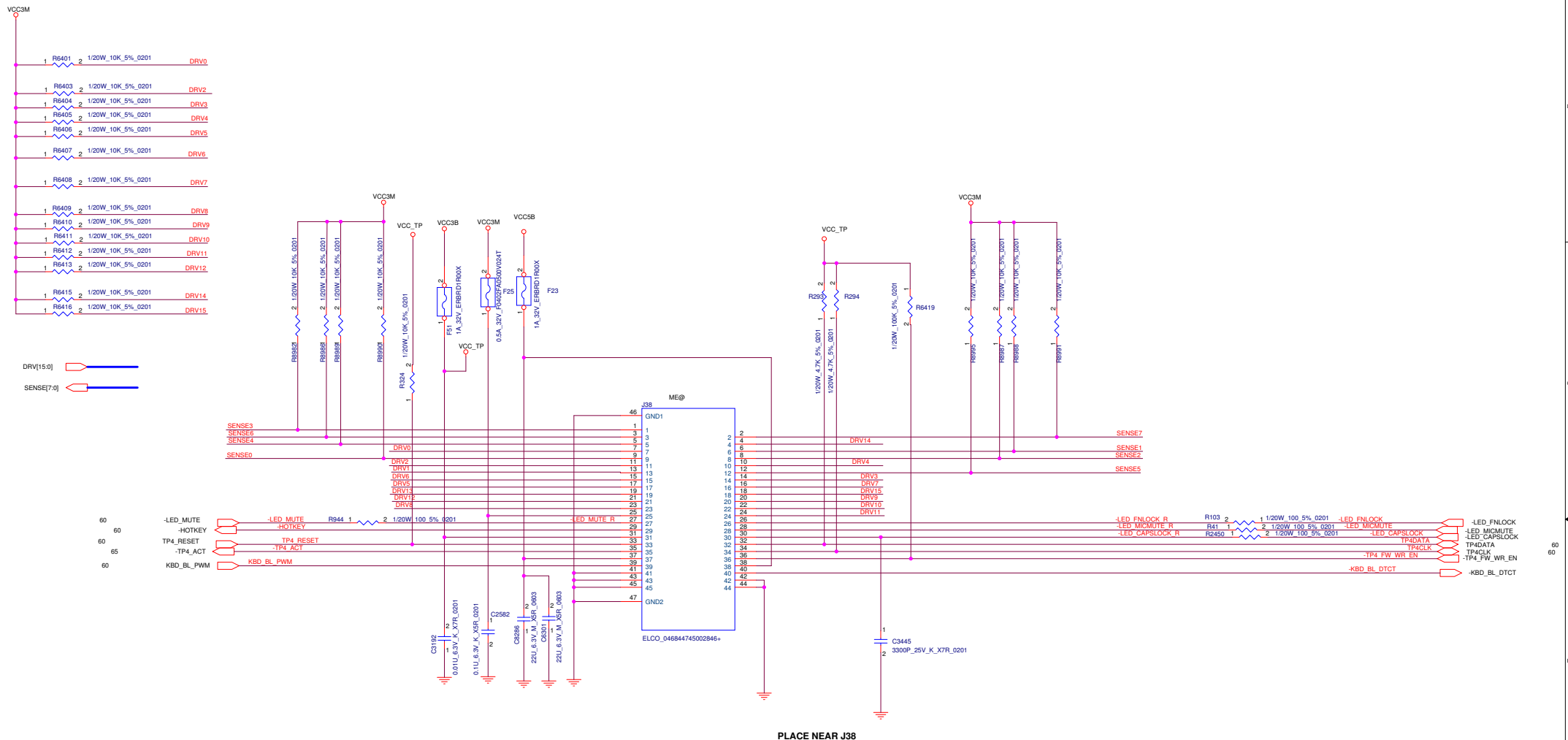
TABLE:EC PLANAR ID2 (GPIO111)

LEVEL	EC_PLANAR_ID2
EVT - ME-SIT-R	HIGH
MFG-SIT-R and later	LOW

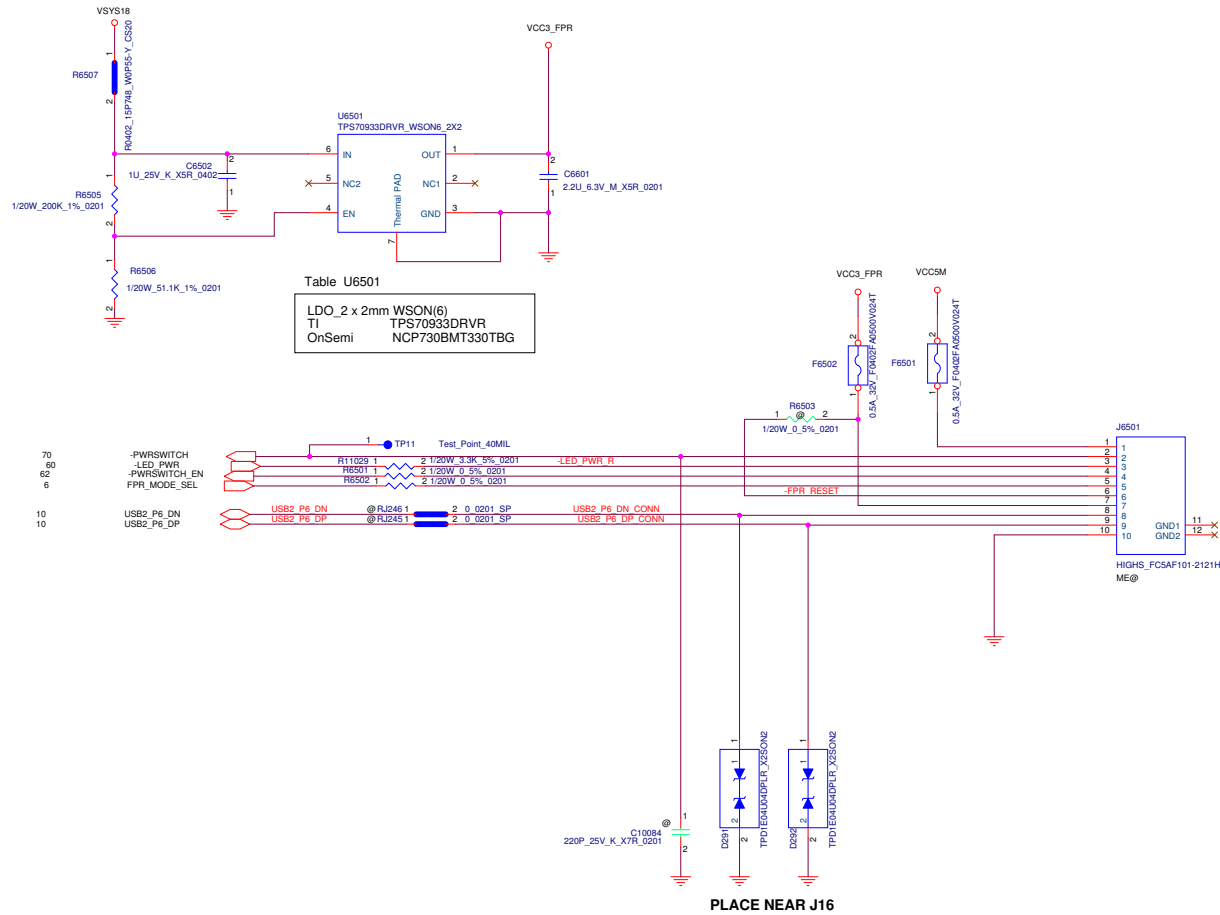
Lenovo

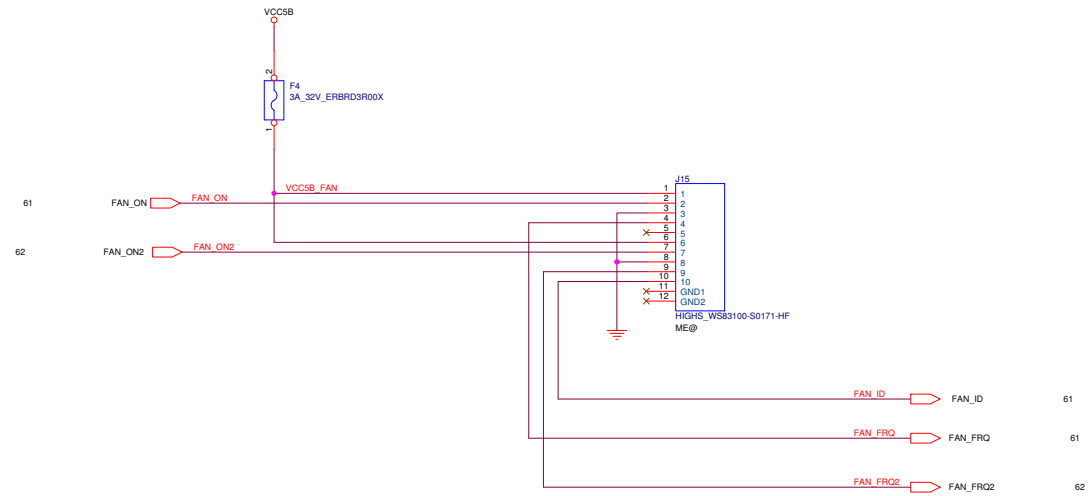
Project Name : Jaguar-2		Title : MEC1723(3/4)	
Size :	Document Number :	Rev : 2.23	
Date: Friday, December 10, 2021		Sheet : 62 of 98	







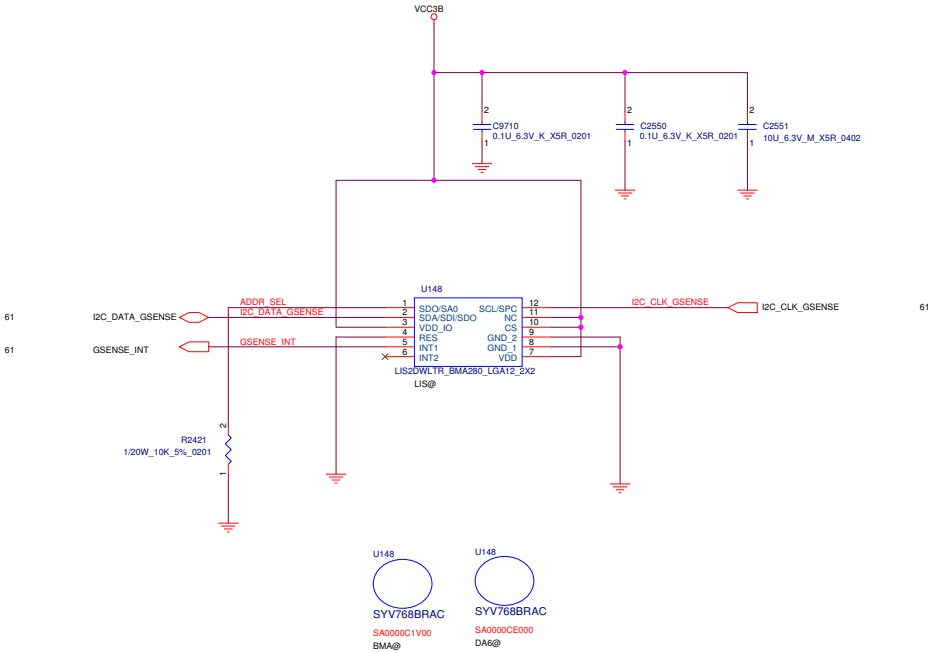




TABLE

	ADDR_SEL	I2C slave address
LIS2DWL	H	19h
	L	18h
BMA422	H	19h
	L	18h
DA6618	H	27h
	L	26h

ST and Bosch I2C address is same but can be identified by Chip\_ID



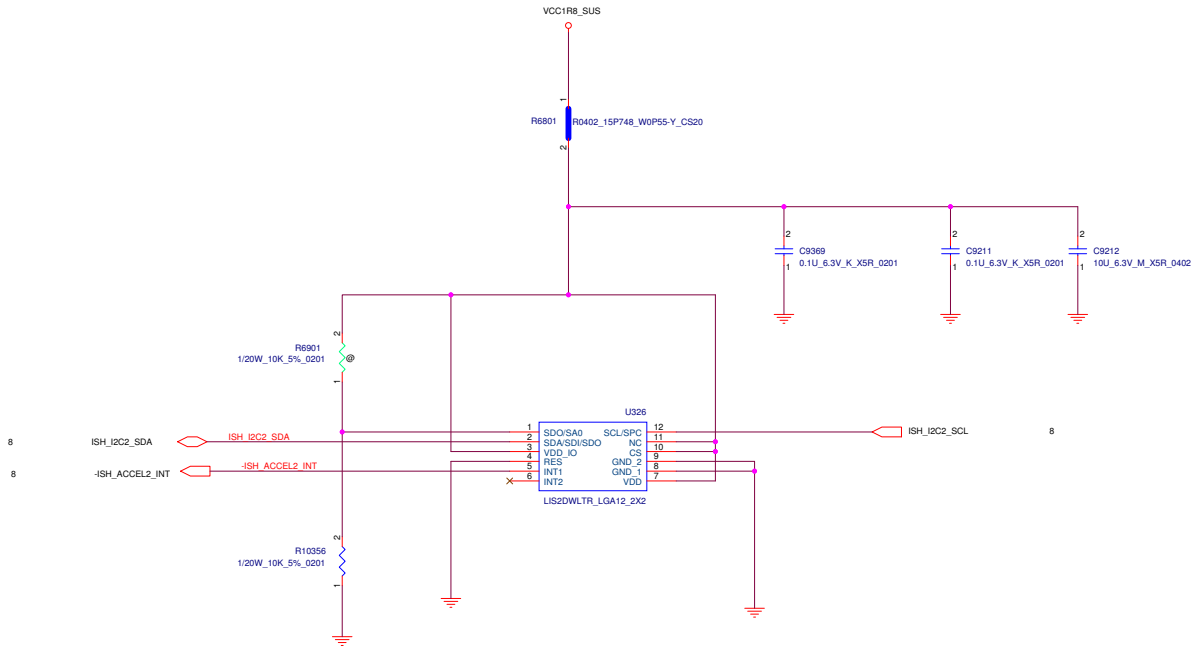
TABLE

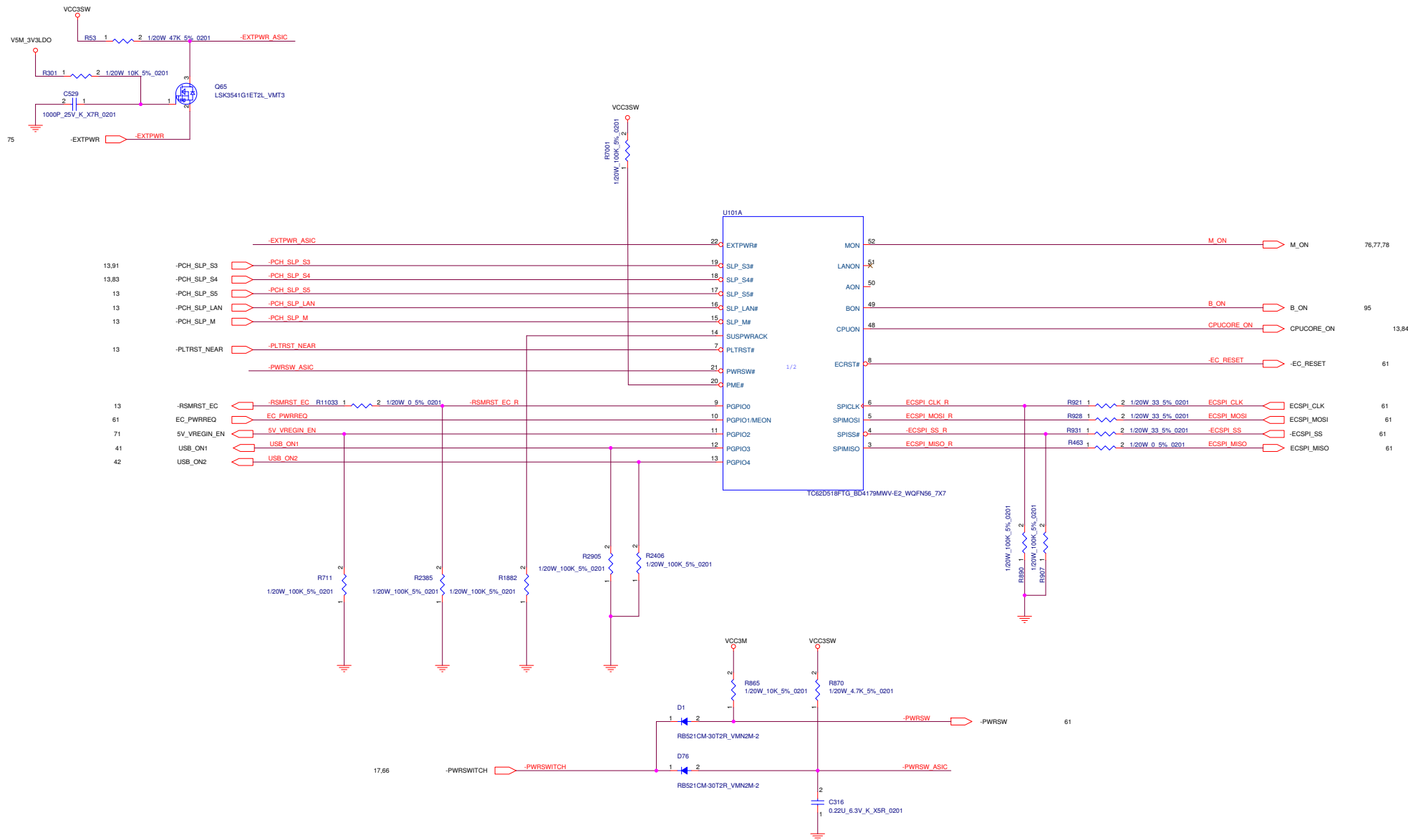
PN	SDO	I2C Address
LIS2DWL	H	19h
	L	18h
BMA422	H	19h
	L	18h

ST and Bosch I2C address is same but can be identified by LUID

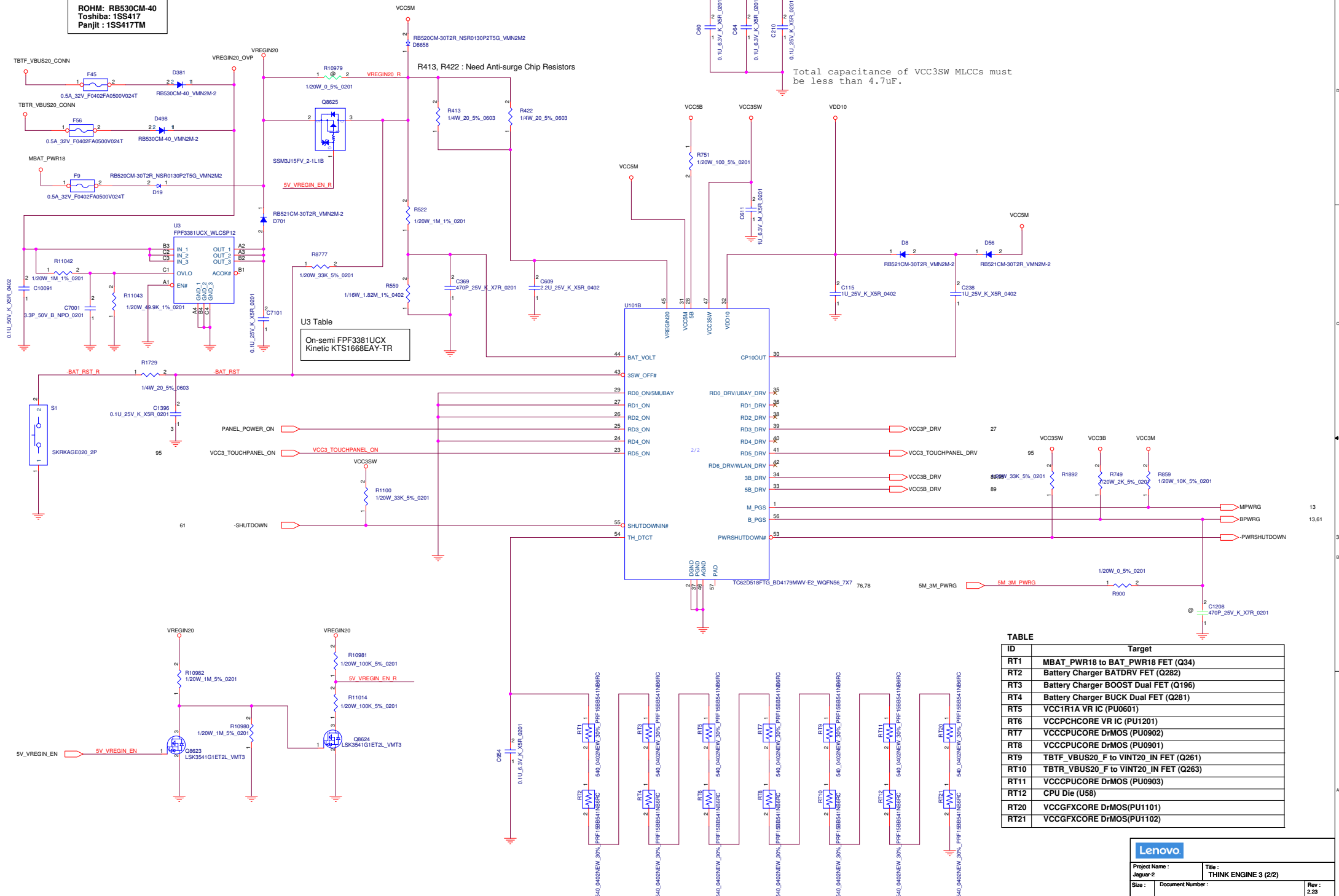
← LOGIC

← LOGIC



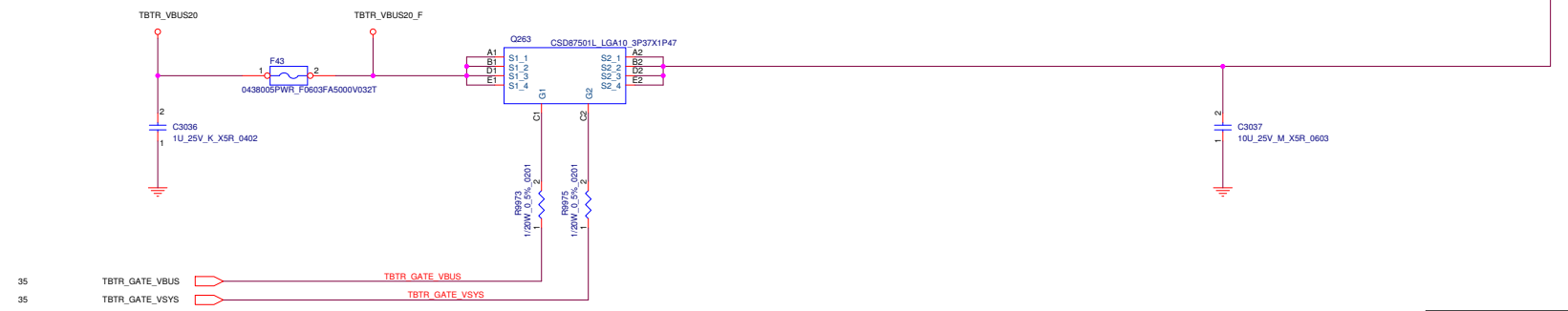
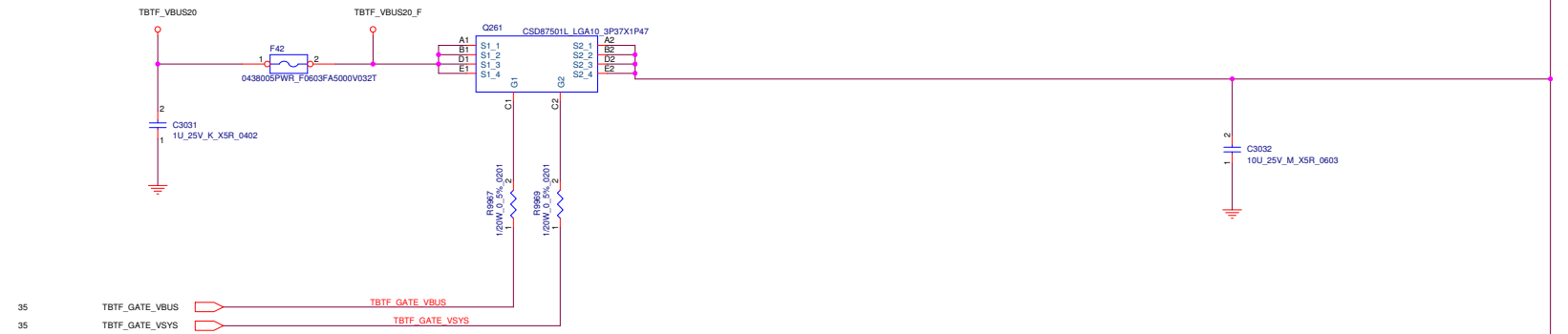
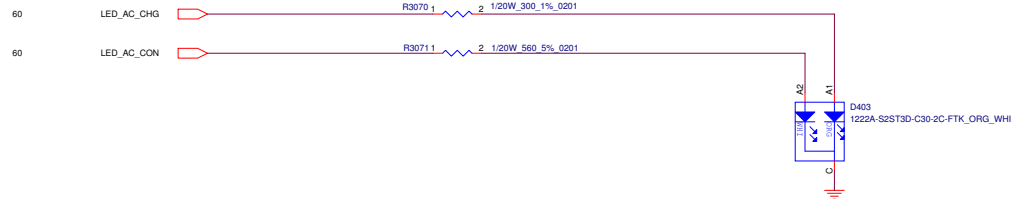


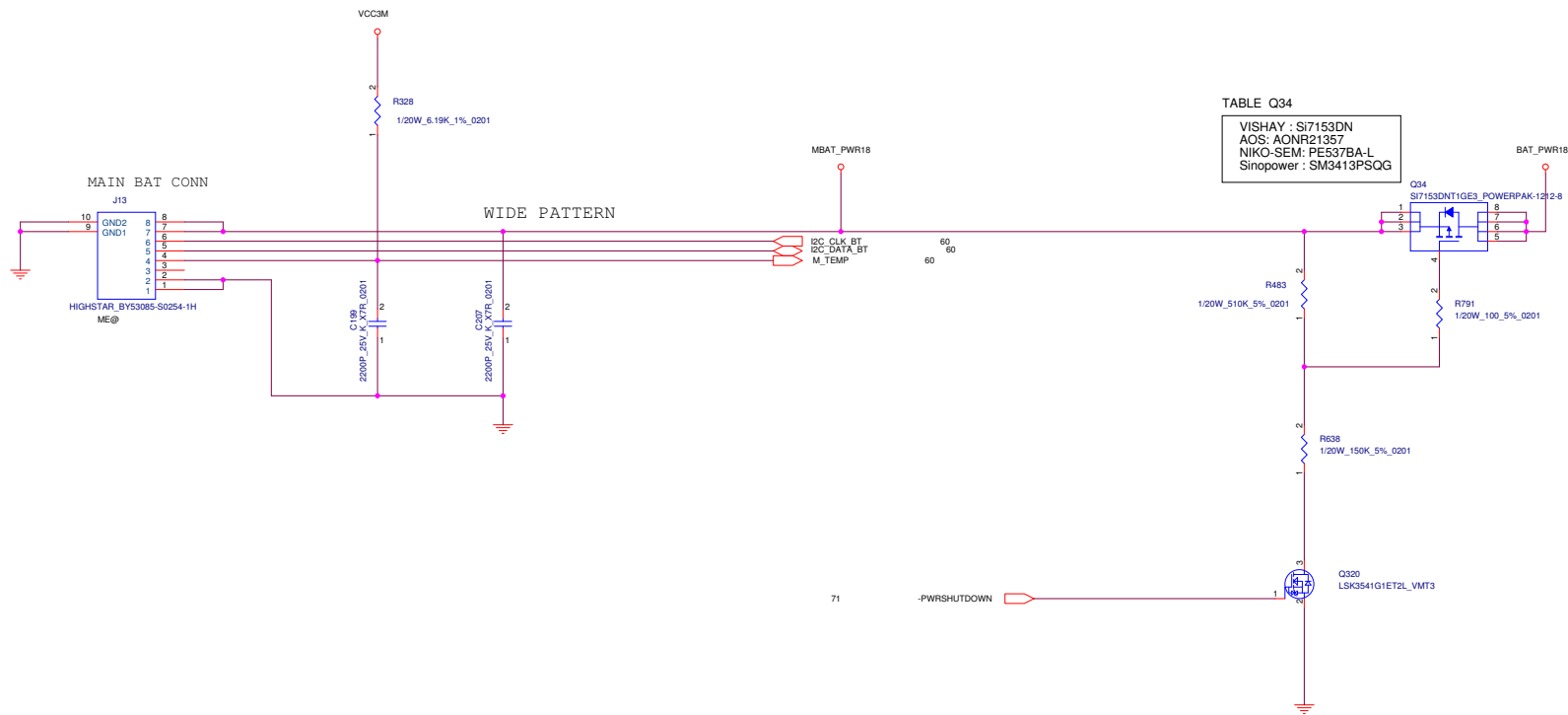
ROHM: RB530CM-40  
Toshiba: 1SS417  
Panjit : 1SS417TM

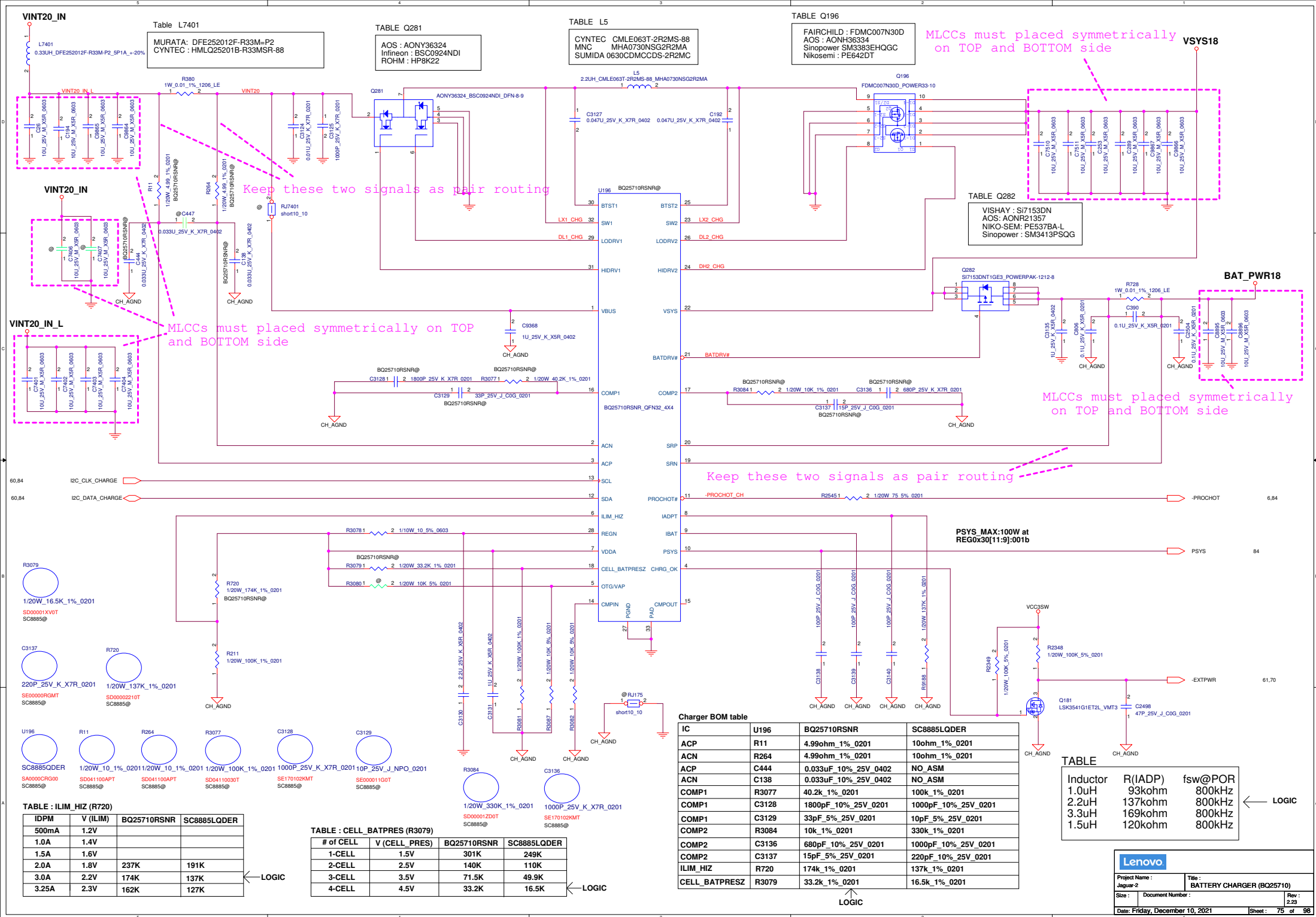


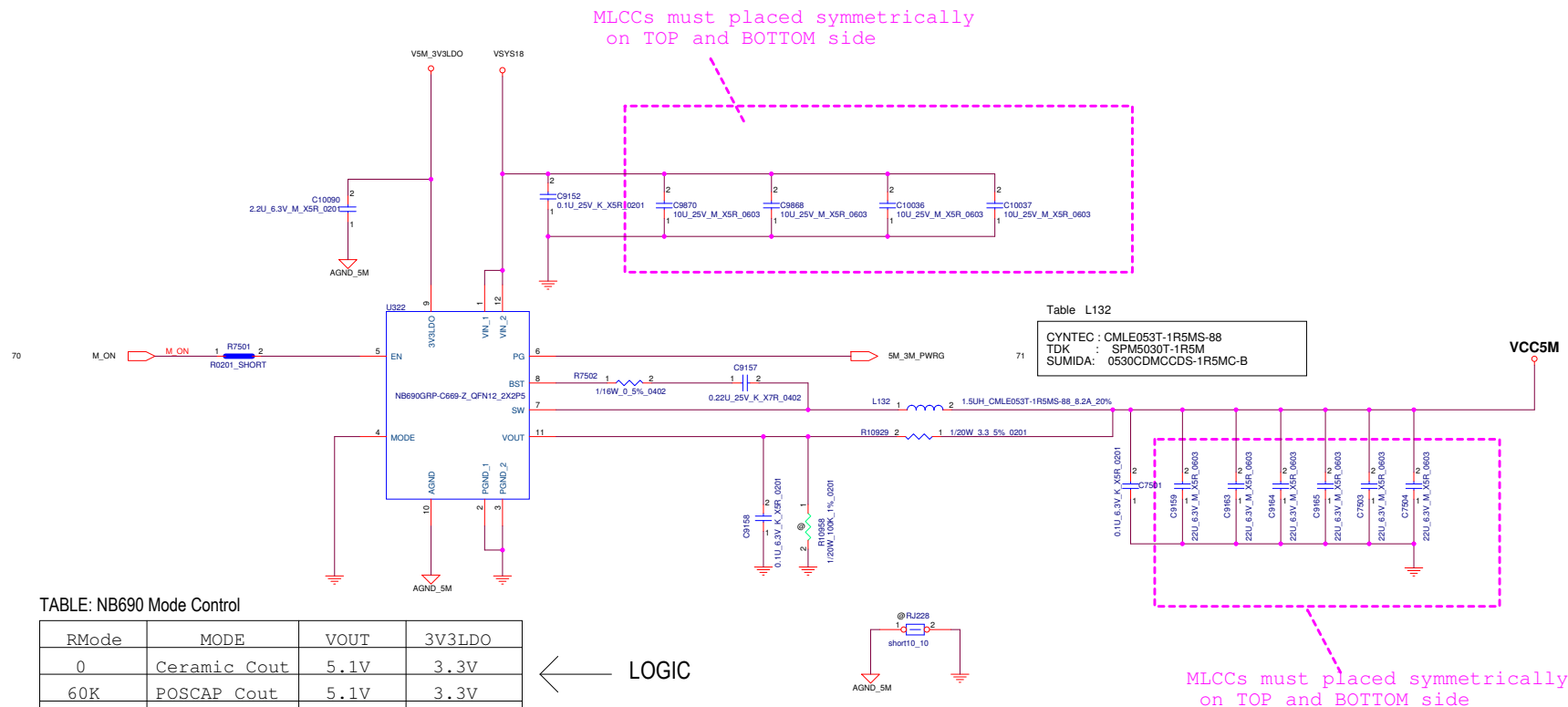
ID	Target
RT1	MBAT_PWR18 to BAT_PWR18 FET (Q34)
RT2	Battery Charger BATDRV FET (Q282)
RT3	Battery Charger BOOST Dual FET (Q196)
RT4	Battery Charger BUCK Dual FET (Q281)
RT5	VCC1R1A VR IC (PU0601)
RT6	VCCPCHCORE VR IC (PU1201)
RT7	VCCCPUCORE DrMOS (PU0902)
RT8	VCCCPUCORE DrMOS (PU0901)
RT9	TBTF_VBUS20_F to VINT20_IN FET (Q261)
RT10	TBTR_VBUS20_F to VINT20_IN FET (Q263)
RT11	VCCCPUCORE DrMOS (PU0903)
RT12	CPU Die (U58)
RT20	VCCGFXCORE DrMOS(PU1101)
RT21	VCCGFXCORE DrMOS(PU1102)











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TABLE3 : CLM Selection

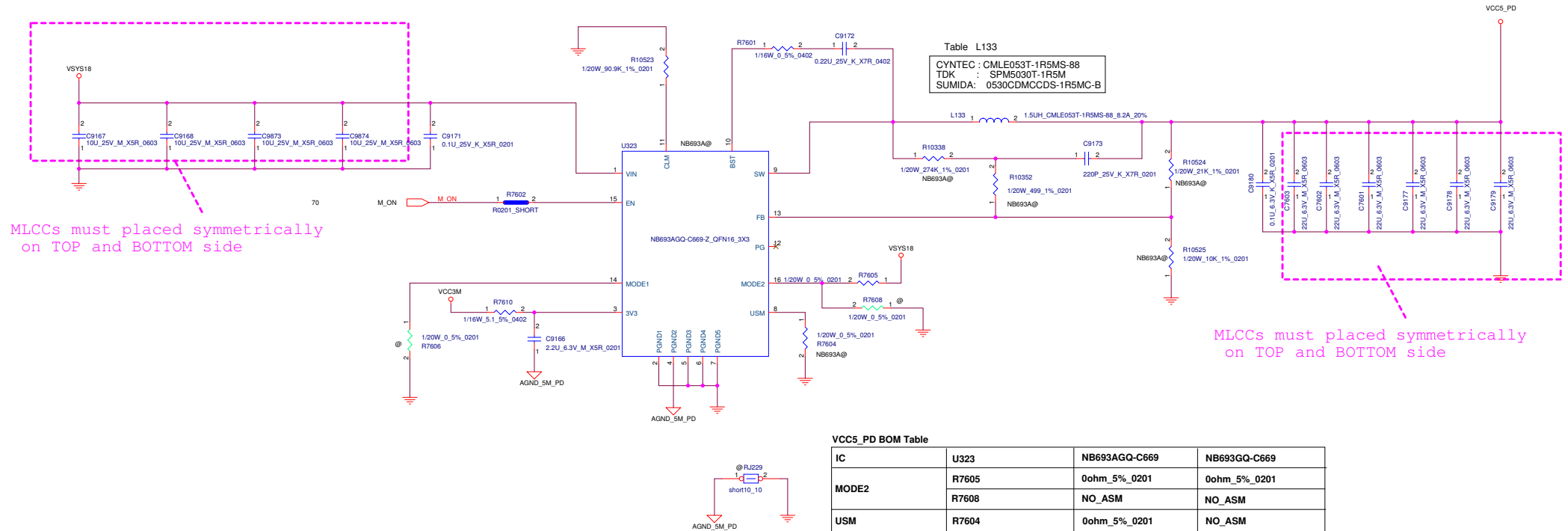
Mode	CLM	Resistor to GND
M1	7A	0
M2	10A	90K
M3	13A	150K
M4	16A	>230K or Float

← LOGIC

TABLE1 : NB693A Mode1 Selection

State	VOUT	Fs	Resistor to GND
M1	Vo<3V,Vref=0.6V	700kHz	0
M2	Vo<3V,Vref=0.6V	1000kHz	90K
M3	Vo>=3V,Vref=1.8V	1000kHz	150K
M4	Vo>=3V,Vref=1.8V	700kHz	>230K or Float

← LOGIC

VCC5\_PD  
5.3V /6.3A

VCC5\_PD BOM Table

IC	U323	NB693AGQ-C669	NB693GQ-C669
MODE2	R7605	0ohm_5%_0201	0ohm_5%_0201
	R7608	NO_ASM	NO_ASM
USM	R7604	0ohm_5%_0201	NO_ASM
FB (R_top)	R10524	21K_1%_0201	301K_1%_0201
FB (R_bot)	R10525	10K_1%_0201	24.3K_1%_0201
SW-FB	R10338	274K_1%_0201	475K_1%_0201
	R10352	499_1%_0201	36.5K_1%_0201

↑  
LOGIC

TABLE 2 : NB693A MODE2 Selection

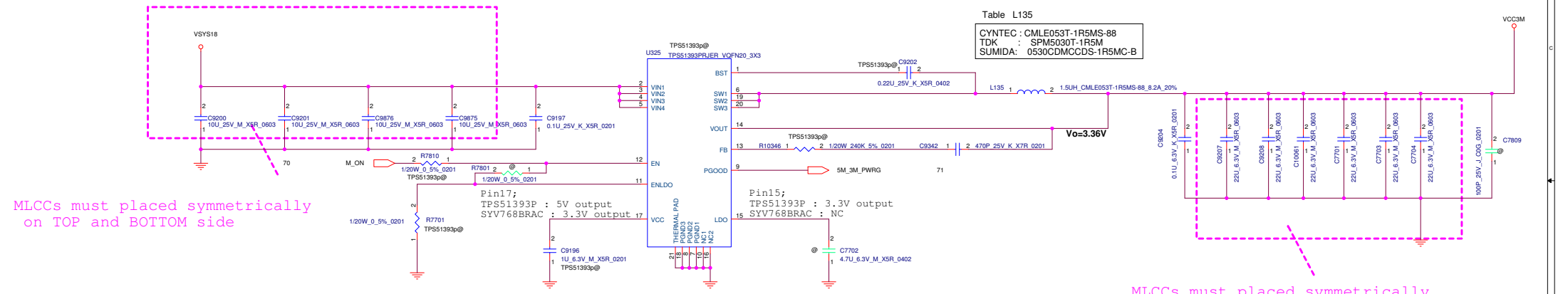
State	VCC	MODE2 set
M1	Internal VCC	0
M2	External VCC	Pull to VIN

← LOGIC

TABLE 4 : USM Selection

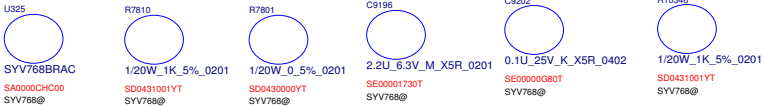
State	USM	Resistor to GND
M1	Y	0
M2	N	Floating

← LOGIC



VCC3M BOM table			
IC	U325	TPS51393P	SYV768BRAC
EN	R7810	0ohm_5%_0201	1k_5%_0201
EN-ENLDO	R7801	NO_ASM	0ohm_5%_0201
ENLDO	R7701	0ohm_5%_0201	NO_ASM
VCC	C9196	1uF_6.3V_X5R_0201	2.2uF_6.3V_X5R_0201
BST	C9202	0.22uF_25V_X5R_0402	0.1uF_25V_X5R_0402
FB	R10346	240k_5%_0201	1k_5%_0201

↑  
LOGIC





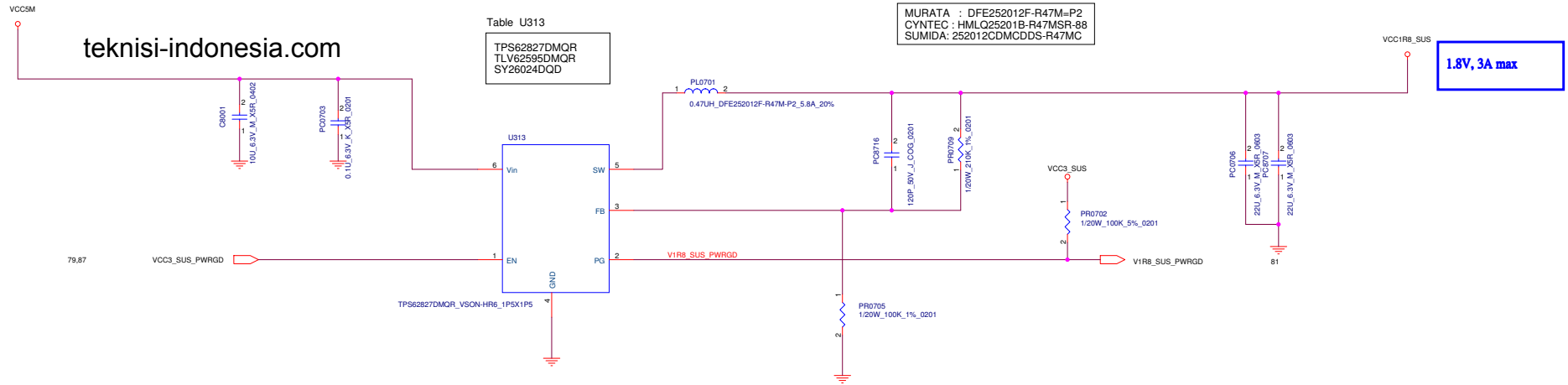
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Table U313

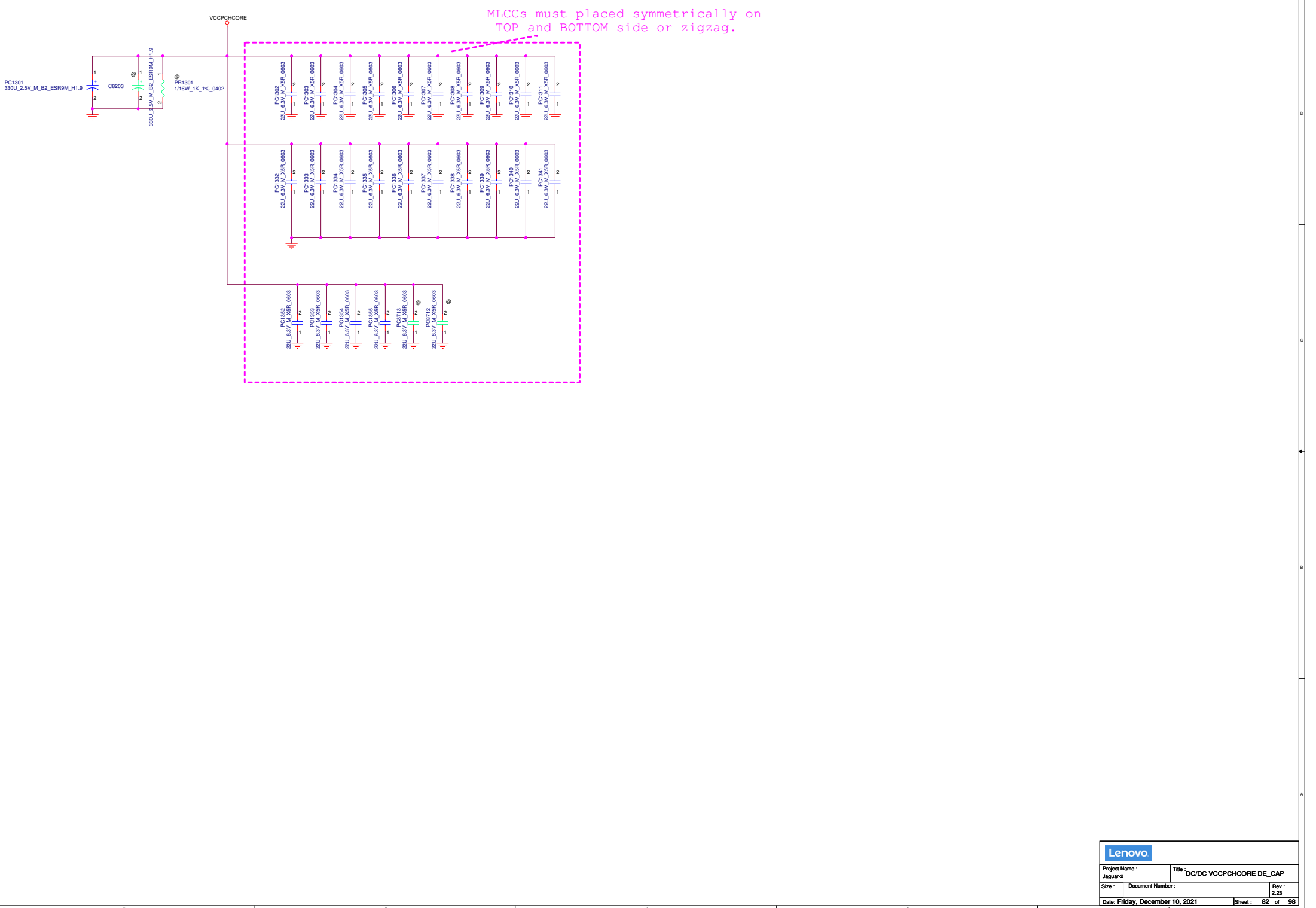
TPS62827DMQR  
TLV62595DMQR  
SY26024DQD

Table PL0701

MURATA : DFE252012F-R47M=P2  
CYNTEC : HMLQ25201B-R47MSR-88  
SUMIDA: 252012CDMCDD-S-R47MC





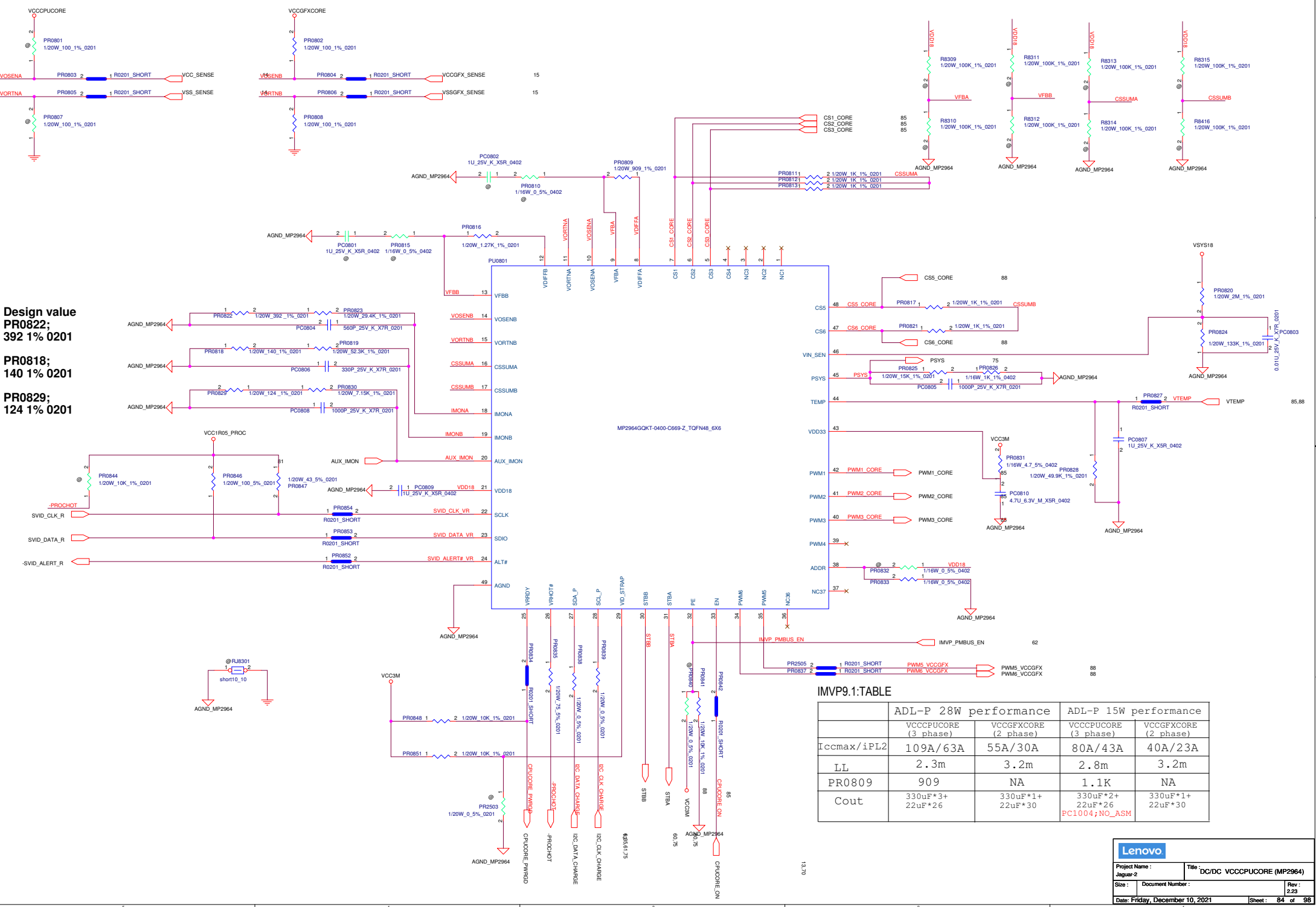




Design value  
PR0822;  
392 1% 0201

PR0818;  
140 1% 0201

PR0829;  
124 1% 0201



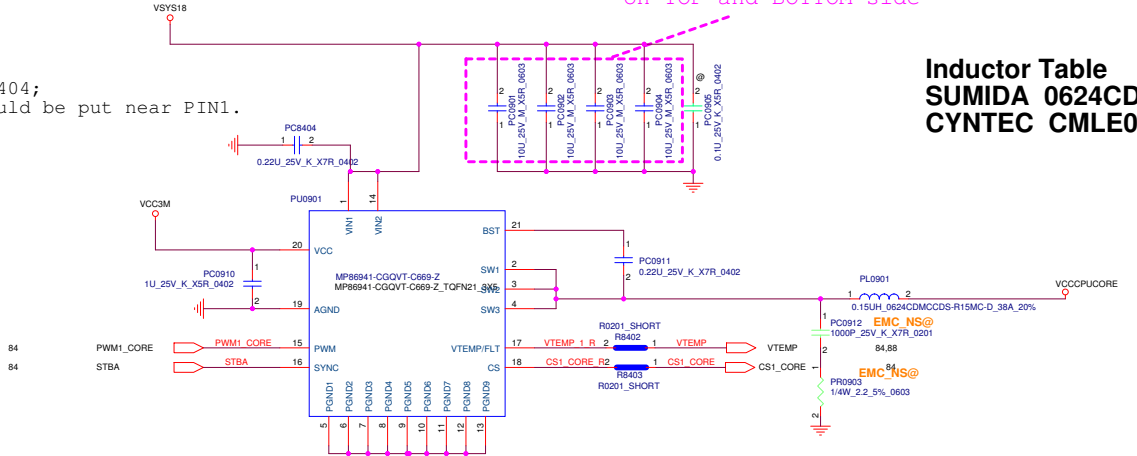
# VCCCPUCORE: PWM1/2/3 TDC:63A IccMax:109A

MLCCs must placed symmetrically  
on TOP and BOTTOM side

PC8404;  
should be put near PIN1.

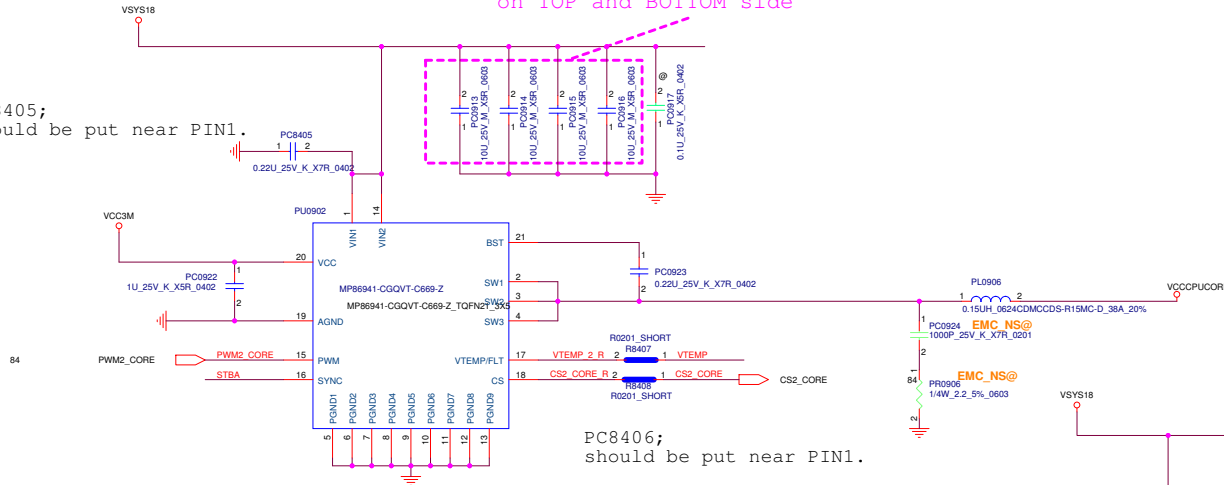
Inductor Table  
SUMIDA 0624CDMCCDS R15MC-D  
CYNTEC CMLE062D-R15MS0R927

Table PU0901,PU0902,PU0903  
MP86941-CGQVT-C669  
MP86941GQVT-C669



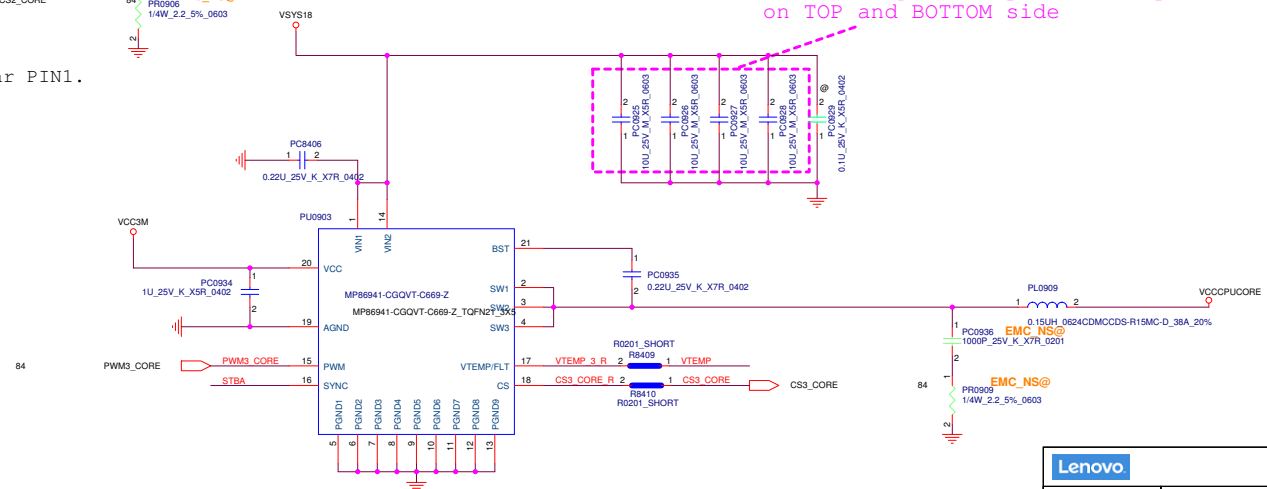
MLCCs must placed symmetrically  
on TOP and BOTTOM side

PC8405;  
should be put near PIN1.

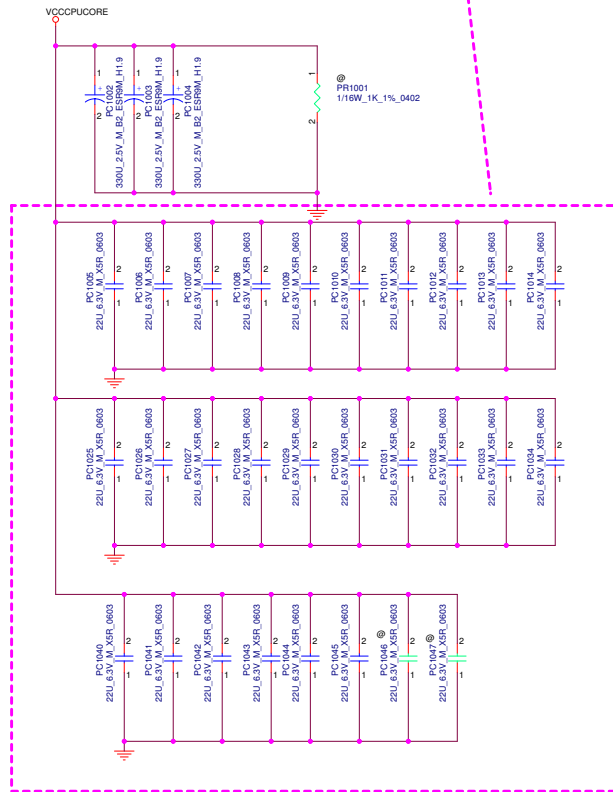


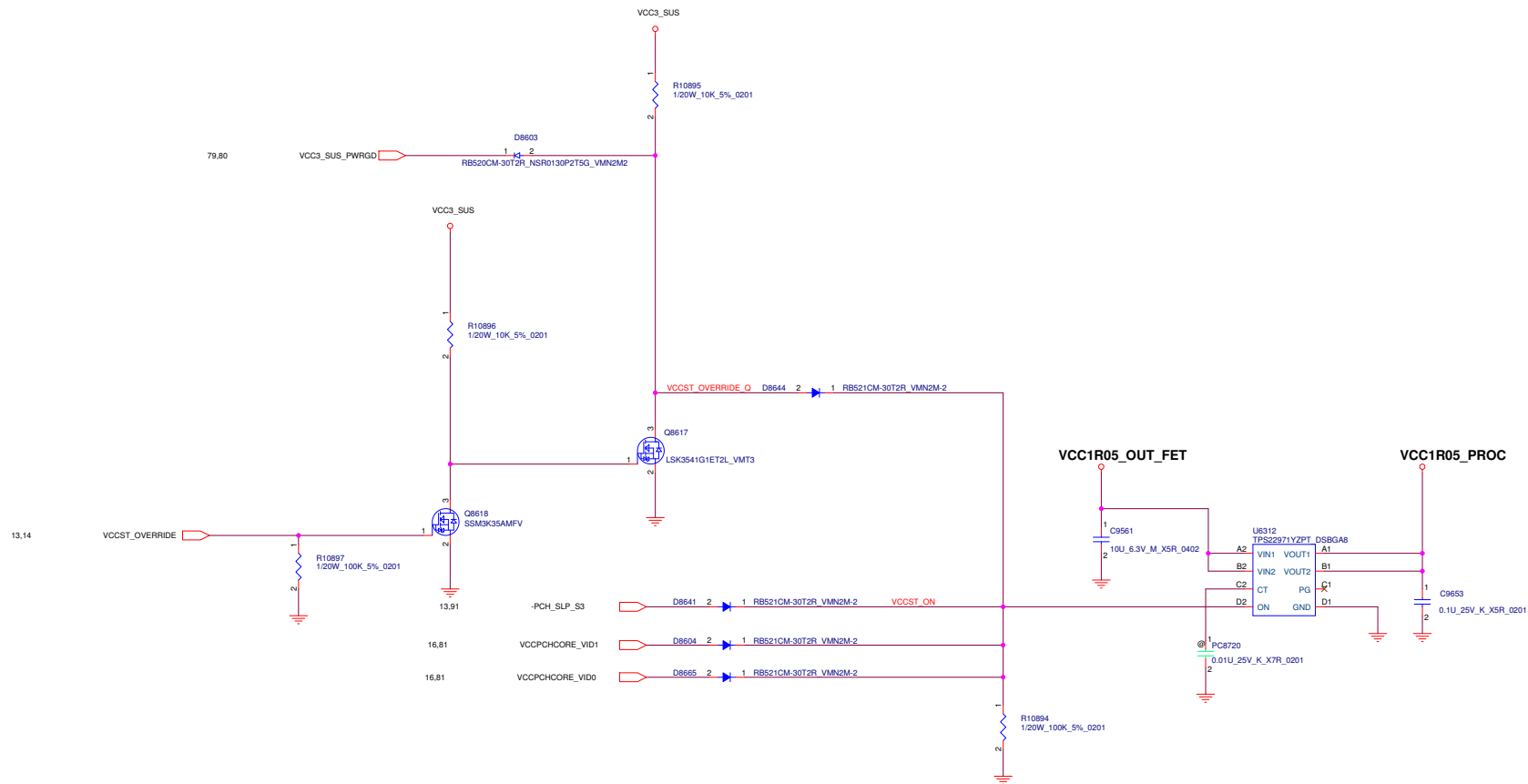
MLCCs must placed symmetrically  
on TOP and BOTTOM side

PC8406;  
should be put near PIN1.



MLCCs must placed symmetrically on  
TOP and BOTTOM side or zigzag.





**VCCGFXCORE: PWM6/5**  
**TDC:30A IccMax:50A**

MLCCs must be placed symmetrically on TOP and BOTTOM side

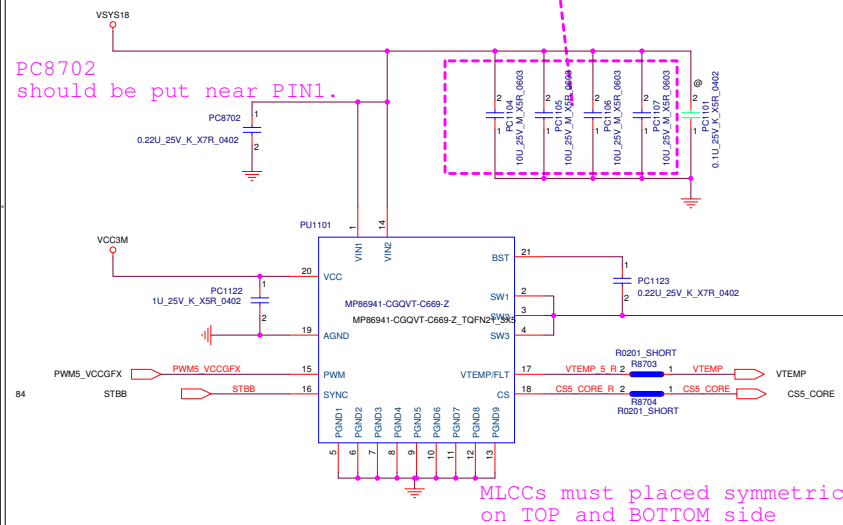


TABLE PL1101

SUMIDA 0624CDMCCDS\_R15MC  
CYNTEC CMLE062D-R15MS0R927

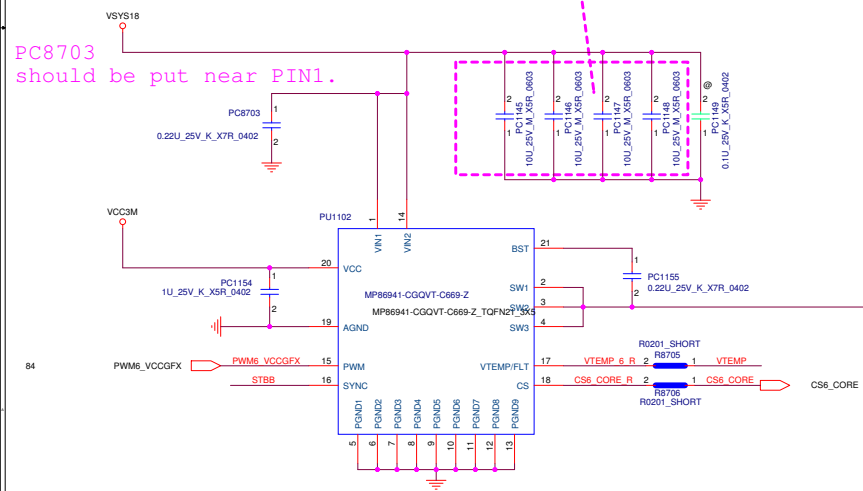
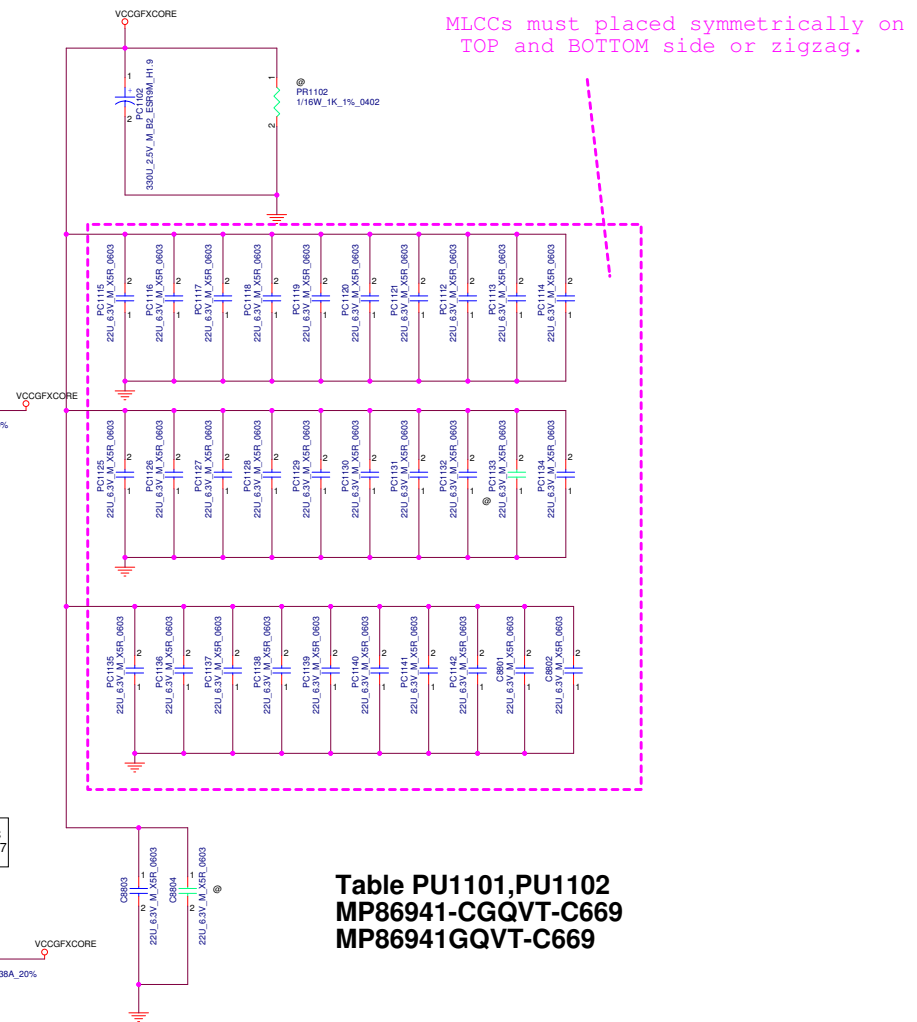


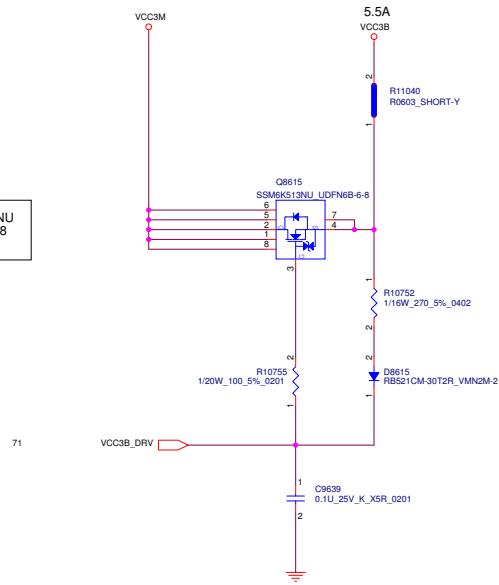
TABLE PL1104

SUMIDA	0624CDMCCDS_R15MC
CYNTEC	CMLE062D-R15MS0R927

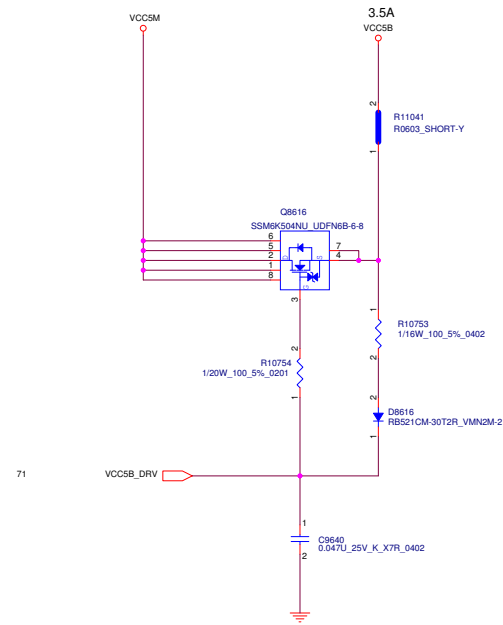


**Table PU1101,PU1102  
MP86941-CGQVT-C669  
MP86941GQVT-C669**

Q8615  
TOSHIBA : SSM6K513NU  
FAIRCHILD : FDMA8878  
AOS : AON2420



Q8616  
TOSHIBA : SSM6K504NU  
AOS : AON2420  
ROHM : RF4E080BNTR  
FAIRCHILD : FDMA8878





60,81  
16  
13,17,70,87

PCHCORE\_PWRGD  
VNN\_CTRL  
-PCH\_SLP\_S3

#### Control Bit Logics:

	LP#	C1	C0	VOUT (V)
VNN_BYPASS	0	X	X	0.7V
	1	0	0	1.05V
	1	0	1	1.05V
	1	1	0	0.78V
	1	1	1	0.7V

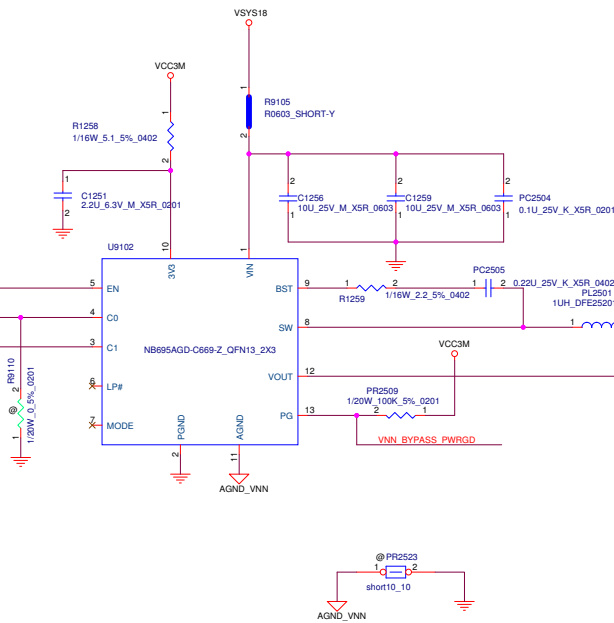


Table PL2501

MURATA: DFE252012F-1R0M=P2  
CYNTEC: HMLQ25201B-1R0MSR-88  
SUMIDA: 252012CDMCCDS-1R0MC

Output Current=0.5A

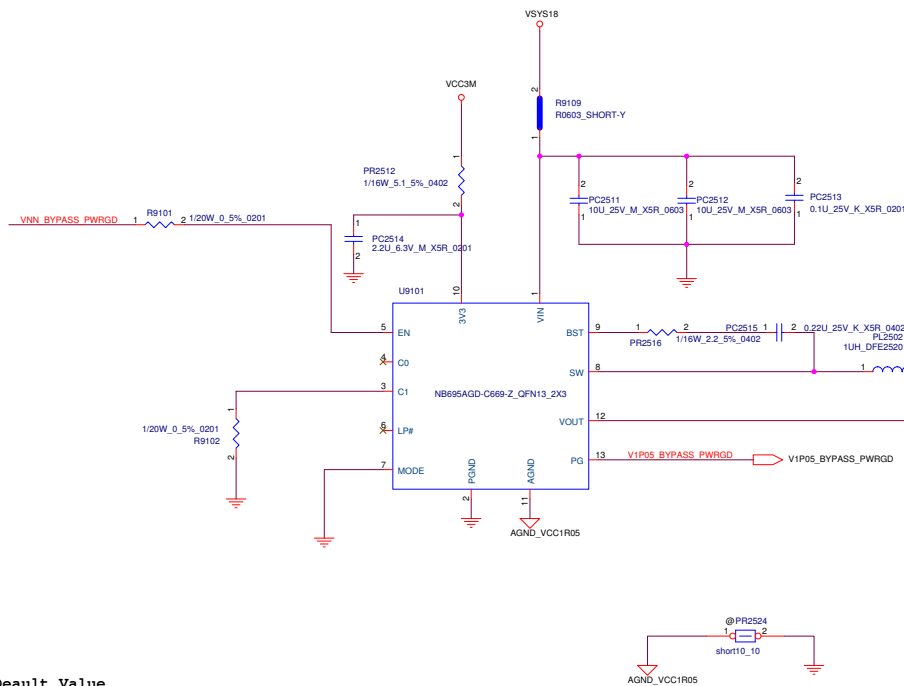


Table PL2502

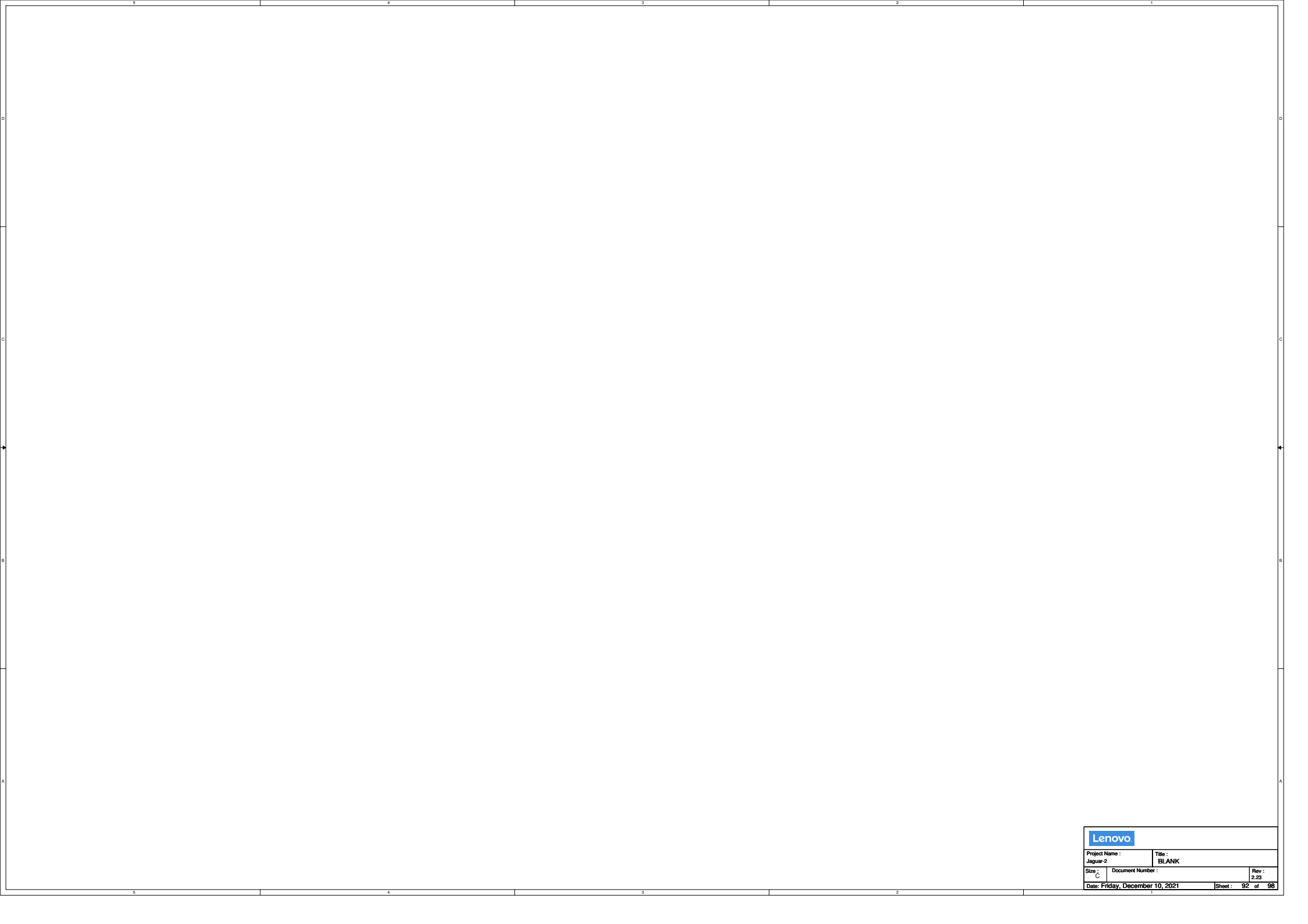
MURATA: DFE252012F-1R0M=P2  
CYNTEC: HMLQ25201B-1R0MSR-88  
SUMIDA: 252012CDMCCDS-1R0MC

Output Current=0.5A

#### Control Bit Logics:

	LP#	C1	C0	VOUT (V)
V1P05_BYPASS	0	X	X	0V
	1	0	0	1.05V
	1	0	1	1.05V
	1	1	0	0.96V
	1	1	1	0.96V

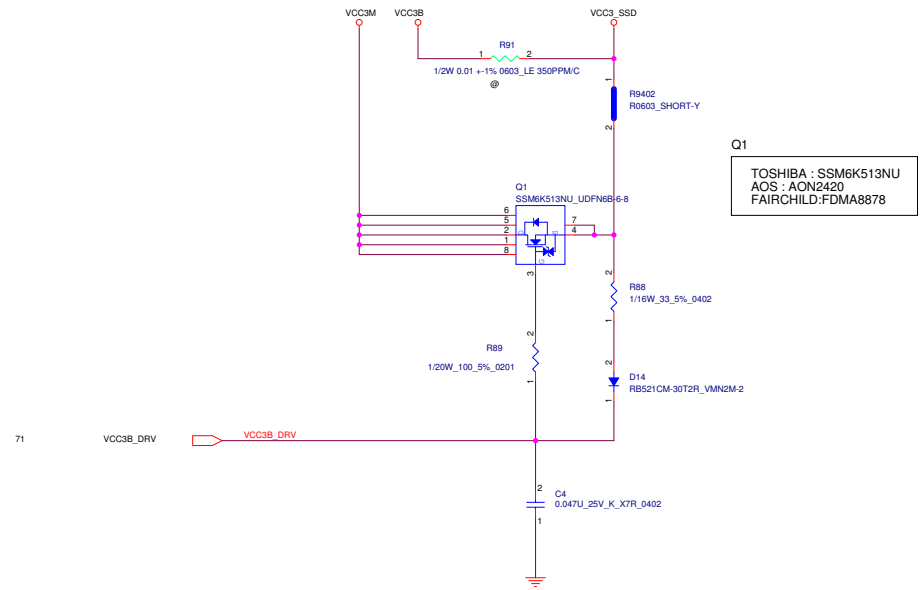
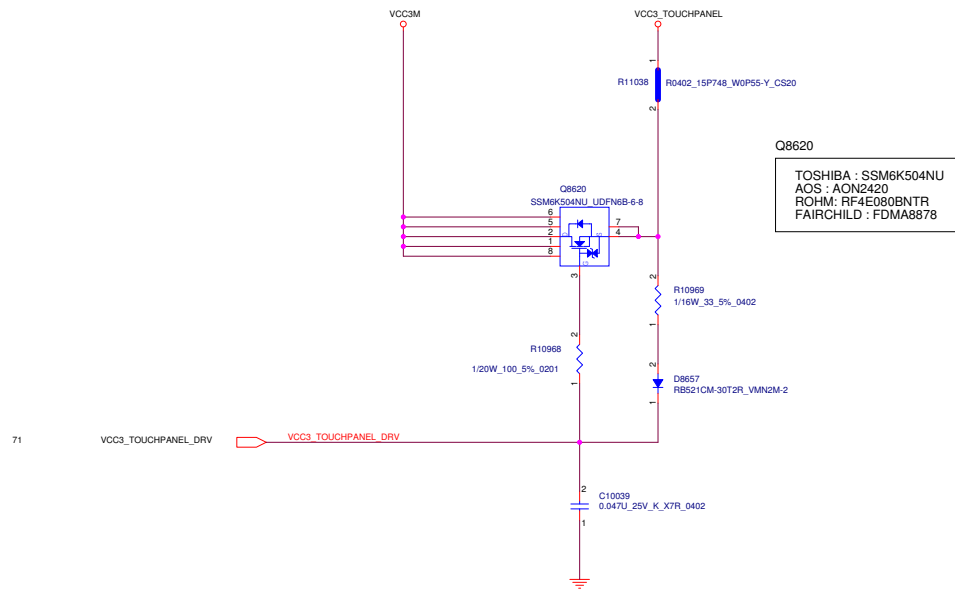
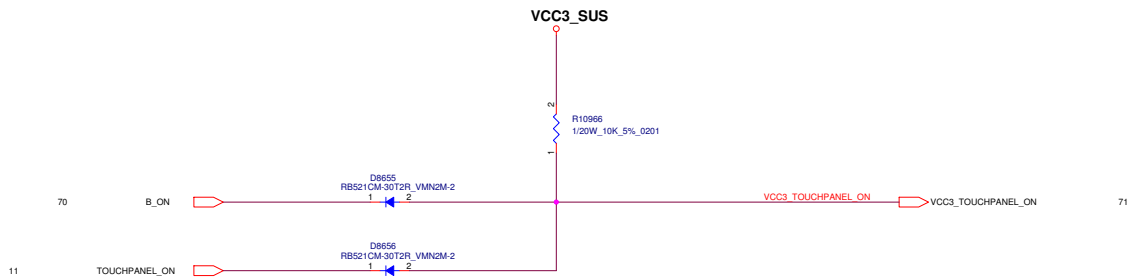
← Deault Value



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Size : C	Document Number :		Rev : 2.23
Date: Friday, December 10, 2021		Sheet : 92 of 98	







FID  
Board Area

